

# Compal Confidential

## YOGA 730 13.3" UMA M/B Schematics Document

Intel KabyLake R Processor with DDR4 Memory Down

Only UMA Design

2017-12-05

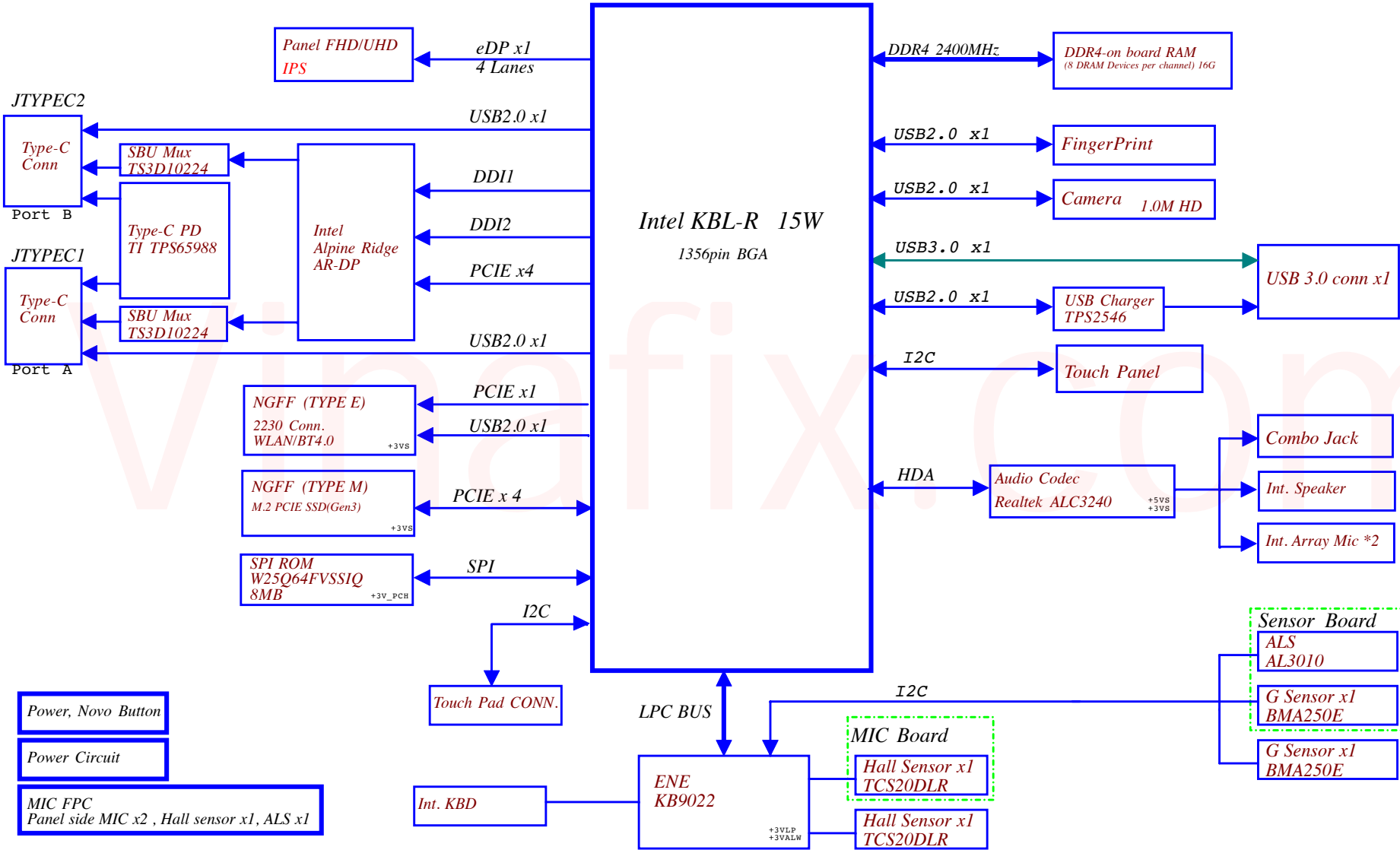
**LA-F571P**

**REV: 1.0**

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# Kabylake-R





power plane State	B+	+5VALW +3VALW +1.8VALW +1.0VALW	+1.2V +2.5V	+5VS +3VS +1.0VS_VCCOPC +VCCCORE +VCCGT +1.0V_VCCST +1.0VS_VCCIO +1.8VS +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Device	Address	Device	Address
Smart Battery	0001 011x 16h	GPU	1001 111x 9Eh

Device	Address
Touch Pad	

	SOURCE	PD	BATT	CHARGER	TP	PCH
EC_SMB_CK1 EC_SMB_DA1	NPCE388 +3VALW	V +3VALW	V +3VALW	V +19V_VIN	X	X
EC_SMB_CK2 EC_SMB_DA2	NPCE388 +3VS	X	X	X	X	V +3VS
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VS	X	X	X	V +3VS	X

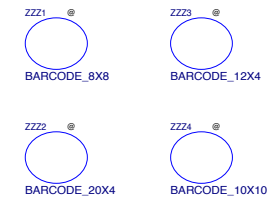
STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF









[illegible]

Port	
1	
2	USB2/3 (Charger)
3	USB2 (Type-C) (JTYPEC1)
4	USB2 (Type-C) (JTYPEC2)
5	Camera
6	Finger print
7	NGFF WLAN+BT
8	

Port	
1	
2	USB2/3
3	USB3 (Type-C) (JTYPECT1)
4	USB3 (Type-C) (JTYPECT1)
5	
6	

Port	Lane	
1	1	Thunderbolt
2	2	
3	3	
4	4	
5	1	
6	1	NGFF WLAN+BT
7	1	SSD
8	2	
9	3	
10	2	
11	1	
12	0	

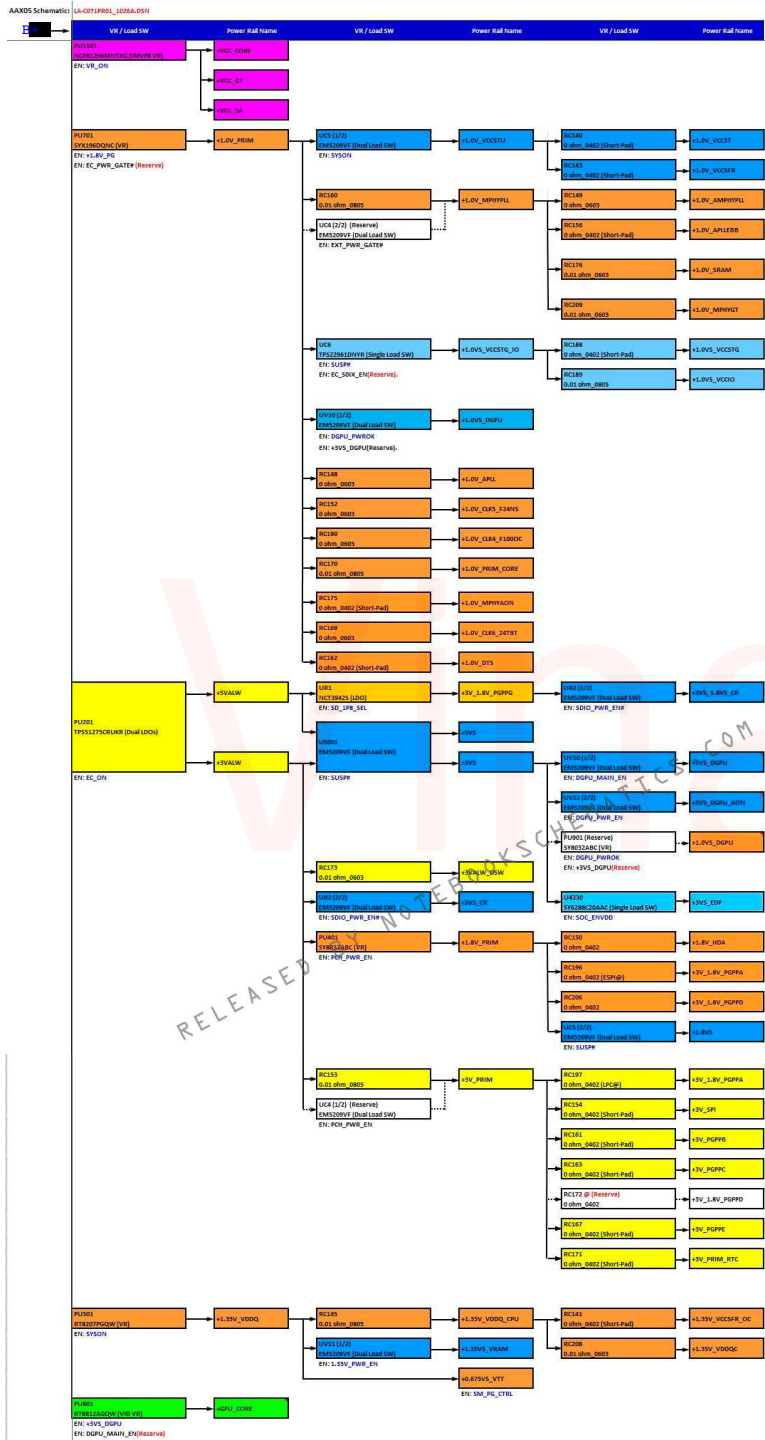


	<b>DDR4 Onboard RAM</b>		
<b>4G</b>	 <p>ZZZ</p> <p>DDR4-Samsung 4G</p> <p>X7676238L10</p>	 <p>ZZZ</p> <p>DDR4-Micron 4G</p> <p>X7676238L11</p>	
<b>8G</b>	 <p>ZZZ</p> <p>DDR4-Samsung 8G</p> <p>X7676238L01</p>	 <p>ZZZ</p> <p>DDR4-Hynix 8G</p> <p>X7676238L02</p>	 <p>ZZZ</p> <p>DDR4-Micron 8G</p> <p>X7676238L03</p>
<b>12G</b>			
<b>16G</b>	 <p>ZZZ</p> <p>DDR4-Samsung 16G</p> <p>X7676238L04</p>	 <p>ZZZ</p> <p>DDR4-Hynix 16G</p> <p>X7676238L05</p>	 <p>ZZZ</p> <p>DDR4-Micron 16G</p> <p>X7676238L06</p>





## CIZY3 -PowerMap\_KBL-U42\_DDR4\_Volume\_NON CS]



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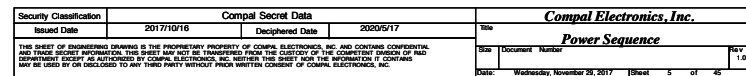
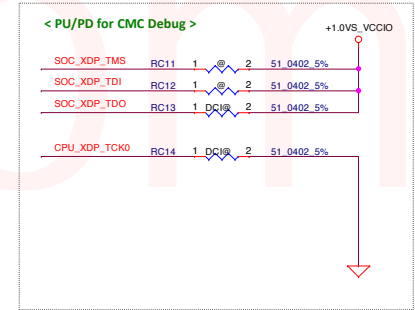
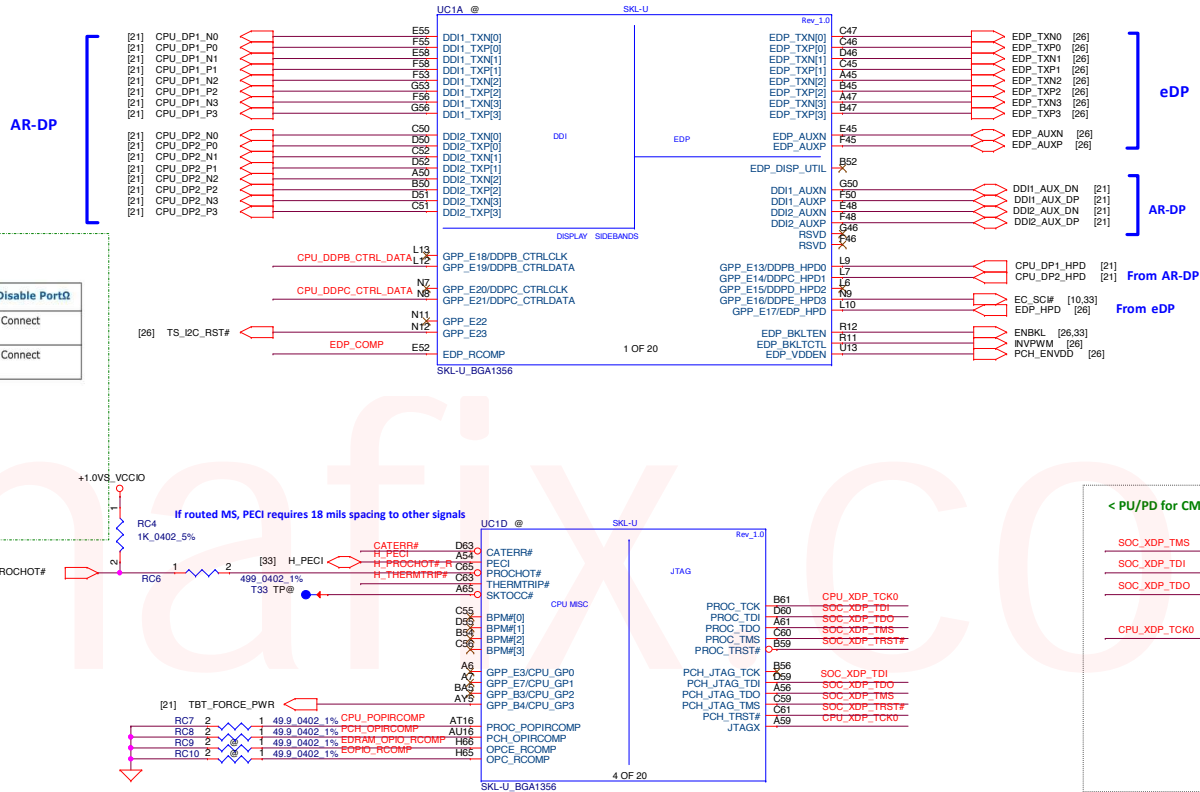
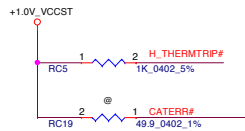
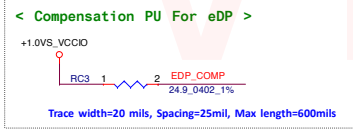
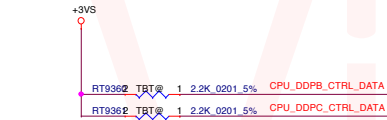




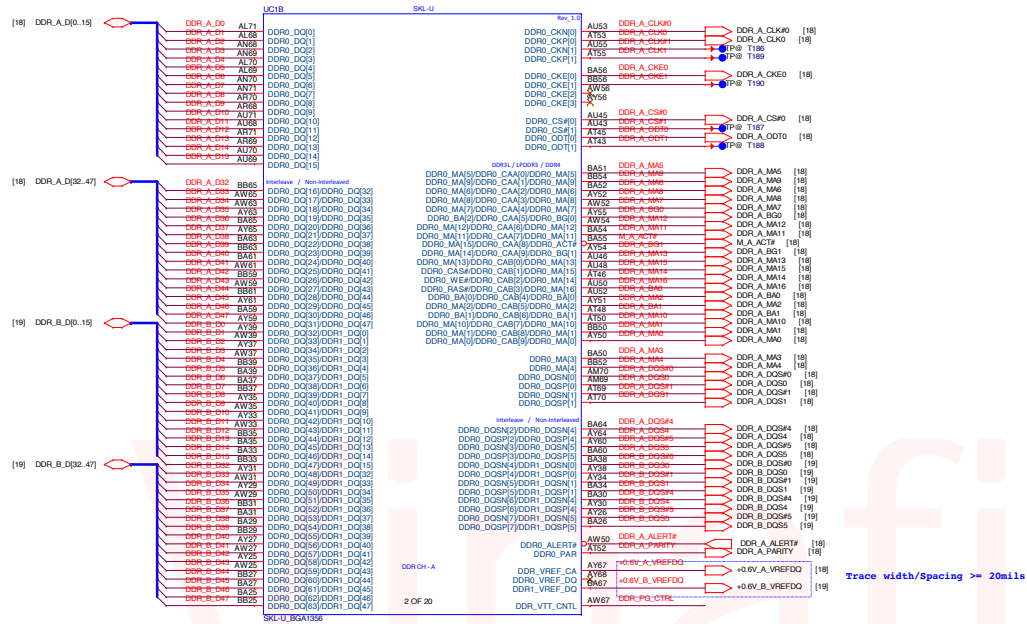
Table 5-9. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port	How to Disable Port
Port 1	DDPB_CTRLDATA	Pull up to 3.3V with 2.2K ohm $\pm 5\%$ resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3V with 2.2K ohm $\pm 5\%$ resistor	No Connect



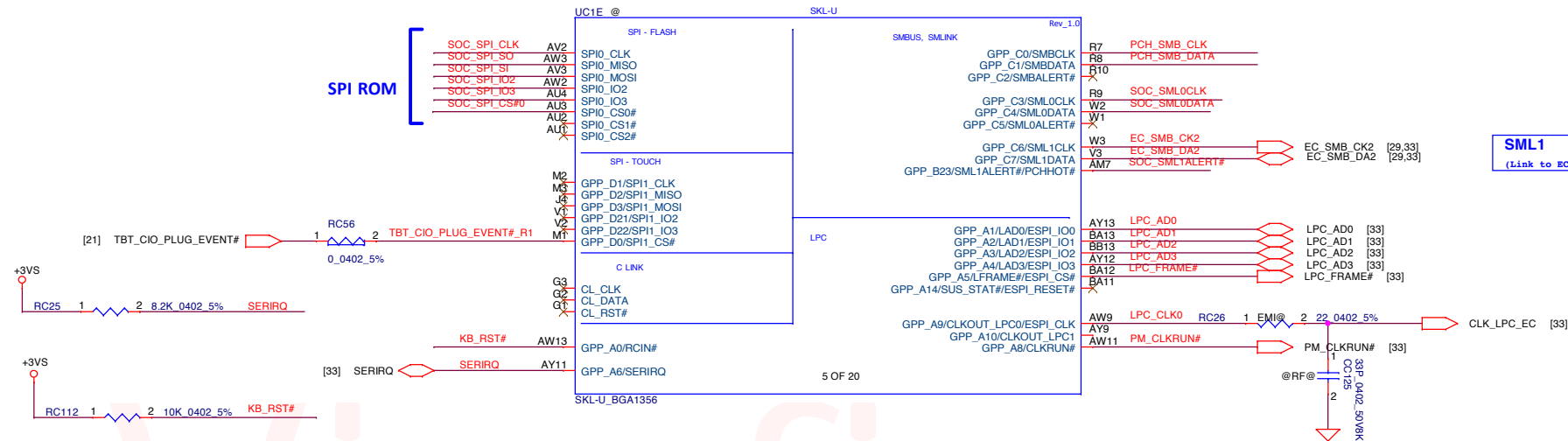


# Non- Interleaved Memory





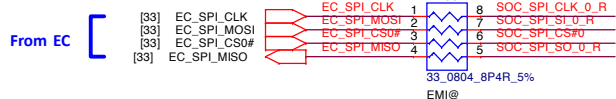
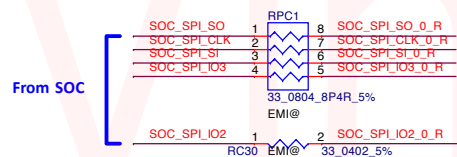
# SPI ROM



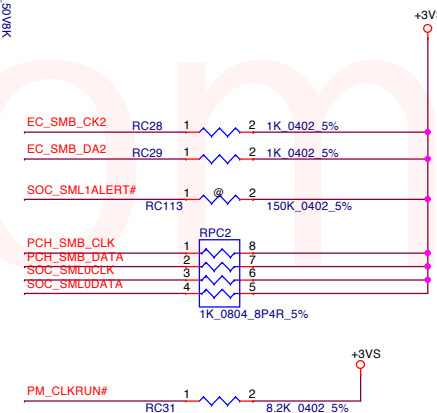
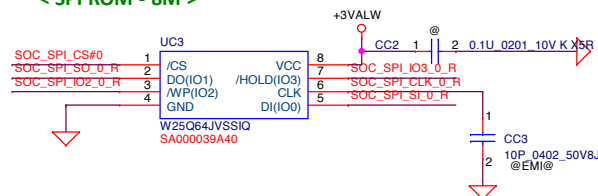
SML0ALERT# (Internal Pull Down):  
eSPI or LPC  
0 = LPC is selected for EC ==> Default  
1 = eSPI is selected for EC

SML1  
(Link to EC, Thermal IC)

RPC1, RPC3 and RC30 are close to UC3



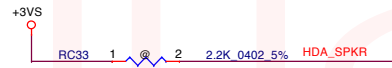
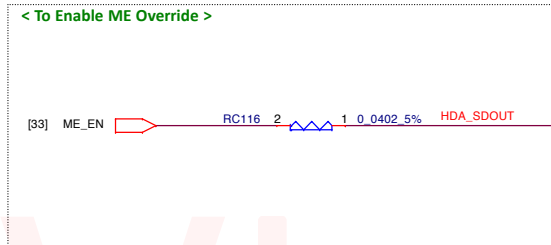
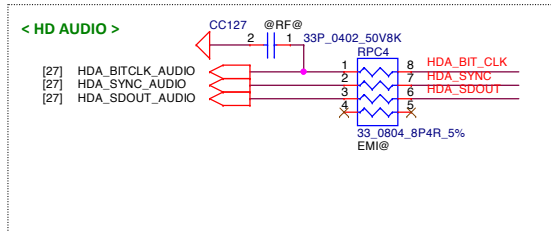
< SPI ROM - 8M >



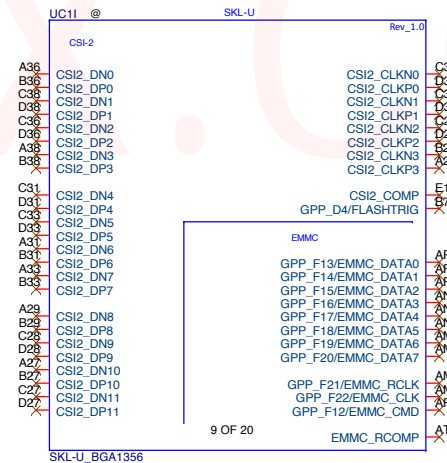
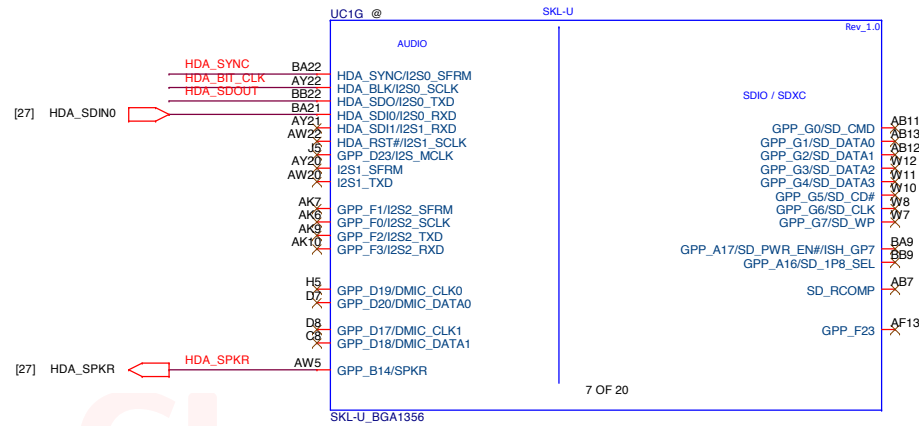
Follow 543016\_SKL\_U\_Y\_PDG\_2\_0

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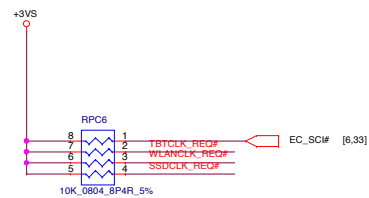


SPKR (Internal Pull Down):  
TOP Swap Override  
0 = Disable TOP Swap mode. ==> Default  
1 = Enable TOP Swap Mode.



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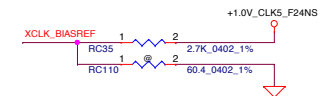
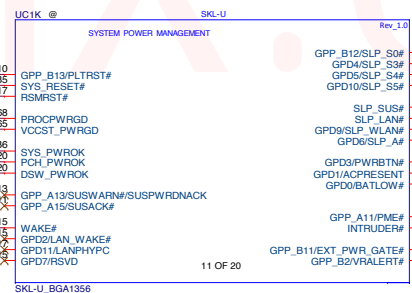
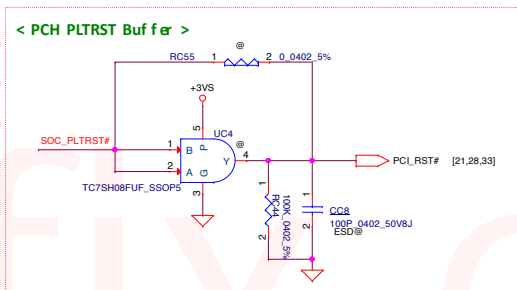
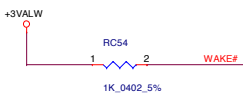
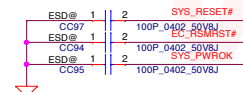
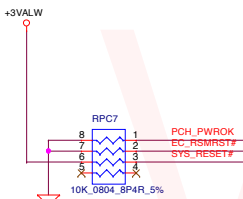
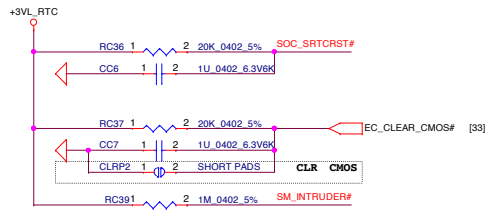
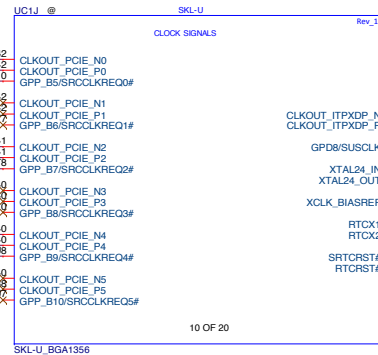




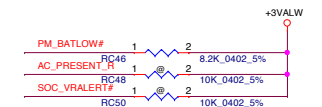
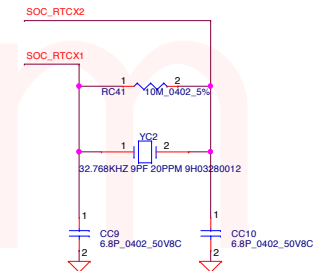
AR-DP

NGFF WL+BT (KEY E)

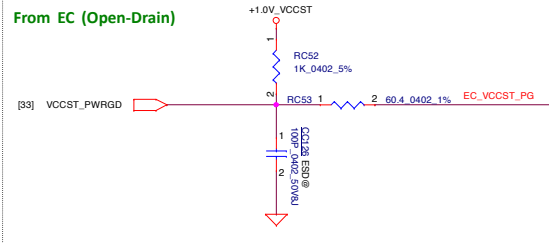
SSD



Follow 546765\_2014W48\_SkyLake\_M0W\_Rev\_1\_0  
Stuff 2.7k ohm(RC35) PU for SkyLake-U  
Stuff 60.4 ohm(RC110) PD for CannonLake-U



From EC (Open-Drain)



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SKL-U(512)CLK.PM.GPIO

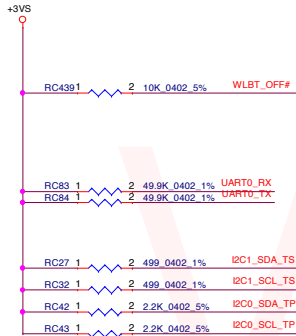
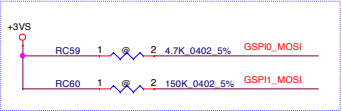
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**GPIO\_MOSI (Internal Pull Down):**  
**No Reboot**  
**0 = Disable No Reboot mode. ==> Default**  
**1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This funct i on is us d f u**  
**when running ITP/XDP.**

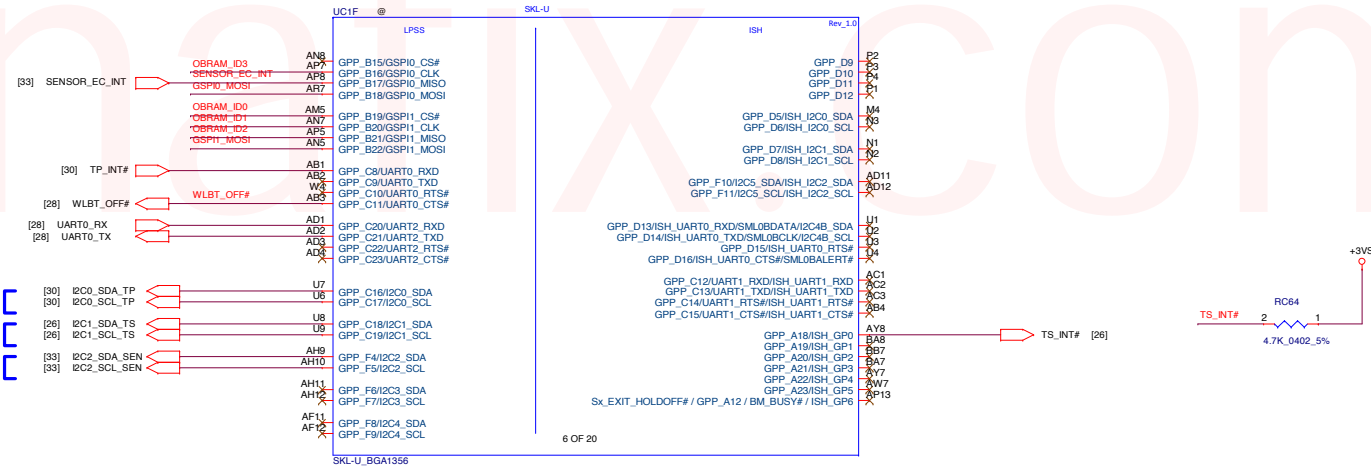
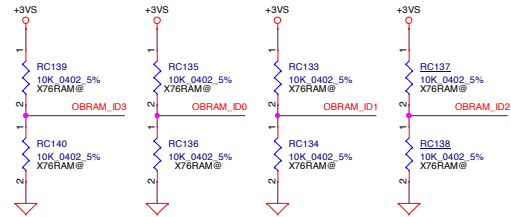
**GPIO1\_MOSI (Internal Pull Down):**

**Boot BIOS Strap Bit**  
**0 = SPI Mode ==> Default**  
**1 = LPC Mode**



**Touch Pad**  
**Touch Panel**  
**Sensor**

Capacity	RAM vendor	GGP_B16	GGP_B19	GGP_B20	GGP_B21
		OBRAM_ID3	OBRAM_ID0	OBRAM_ID1	OBRAM_ID2
4GB	Samsung K4A8G165WC-BCTD	0	0	0	0
	Micron MT40A512M16LY-075:E	0	0	0	1
	N/A	0	0	1	0
8GB	Samsung K4A8G165WC-BCTD	0	0	1	1
	Micron MT40A512M16LY-075:E	0	1	0	0
	Hynix H5AN8G6NAFR-UHC	0	1	0	1
16GB	Samsung K4AAG165WB-MCTD	0	1	1	0
	Micron MT40A1G16WBU-083E:B	0	1	1	1
	Hynix H5ANAG6NAMR-UHC	1	0	0	0
8GB 2400 MHz	Samsung K4A8G165WC-BCRC	1	0	0	1
	Micron MT40A512M16JY-083E:B	1	0	1	0
16GB 2400 MHz	Samsung K4AAG165WB-MCRC	1	0	1	1
	N/A	1	1	0	0
	N/A	1	1	0	1

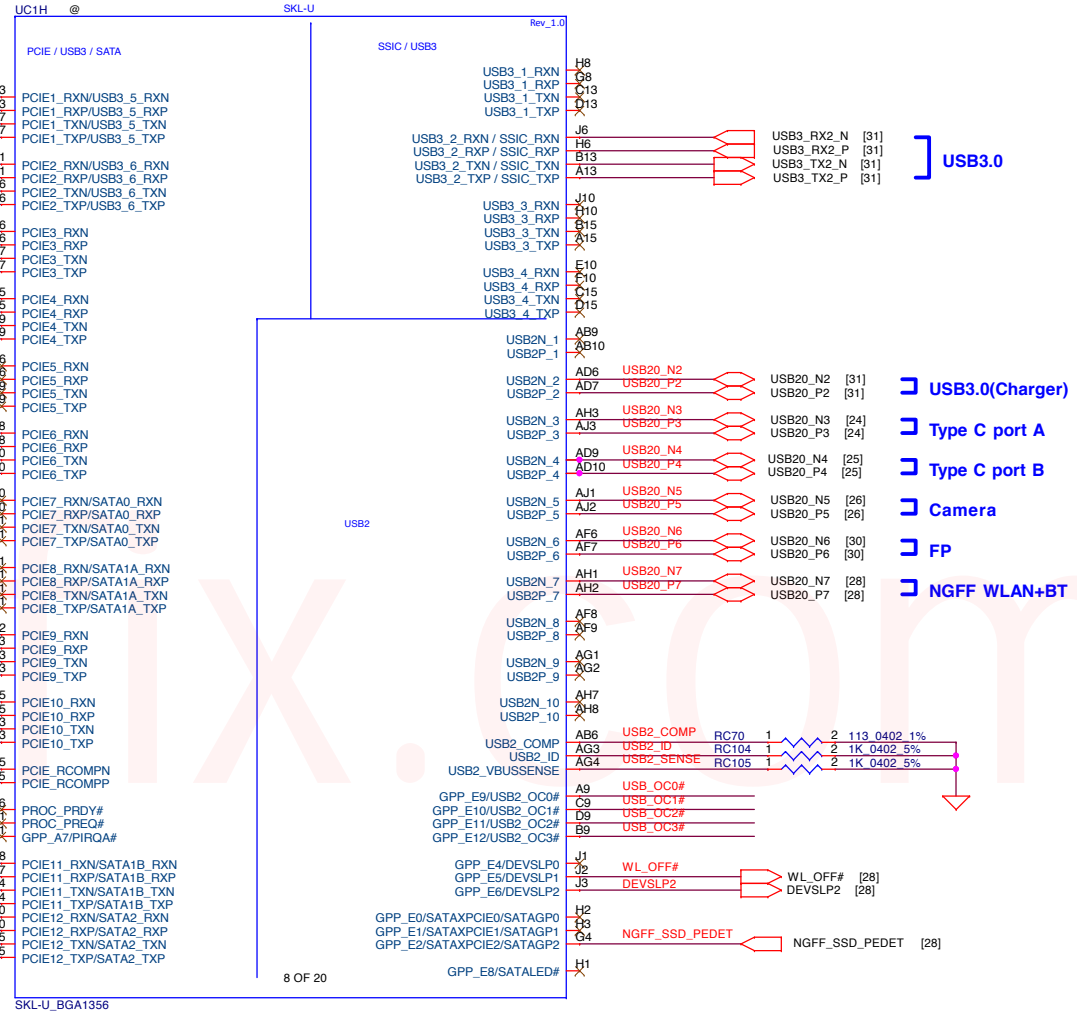




AR-DP

NGFF WLAN+BT

SSD



USB3.0

USB3.0(Charger)

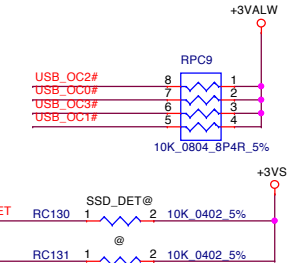
Type C port A

Type C port B

Camera

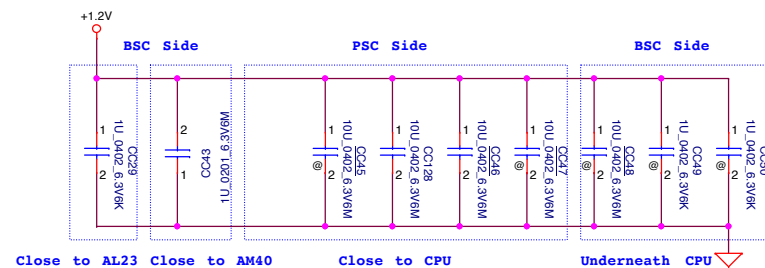
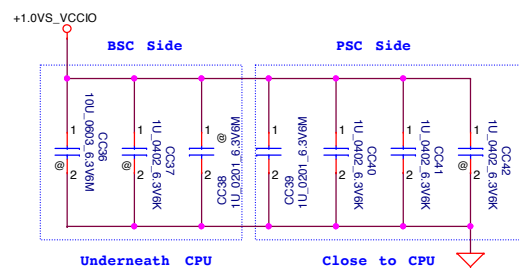
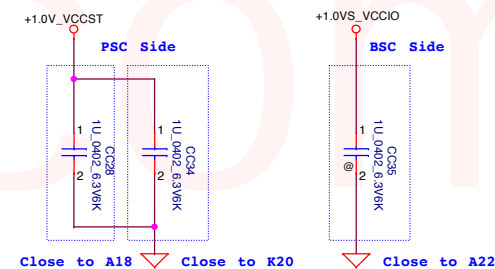
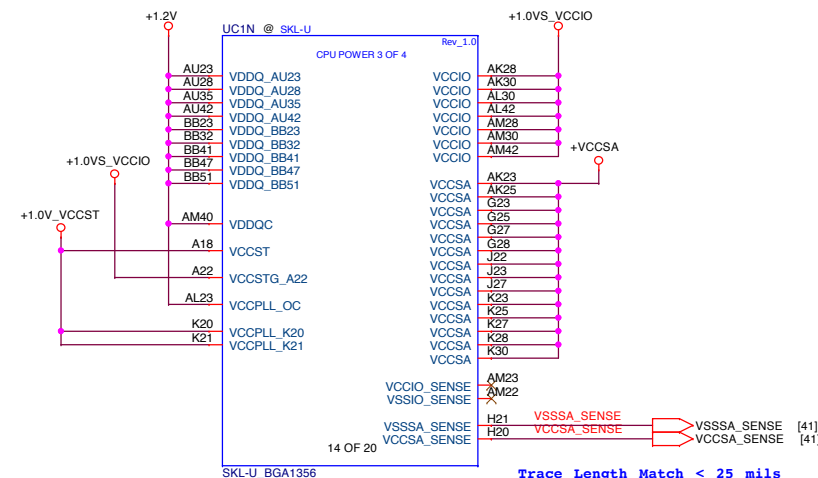
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NGFF WLAN+BT



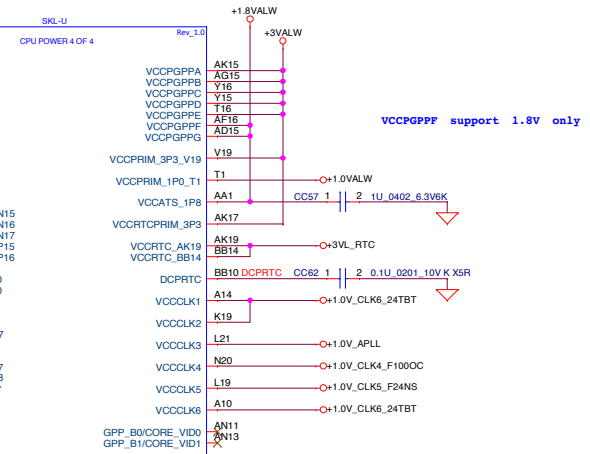
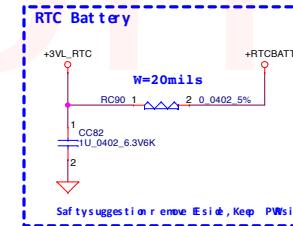
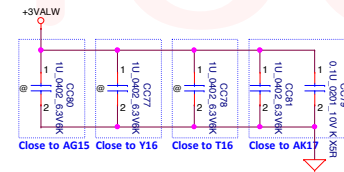
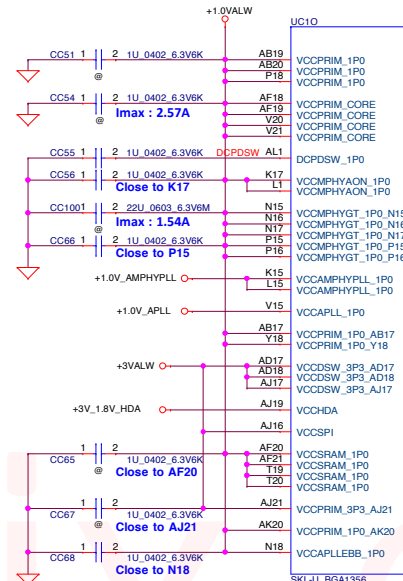
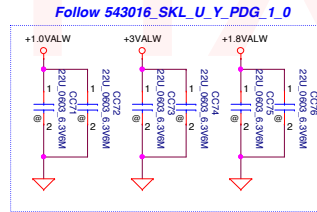
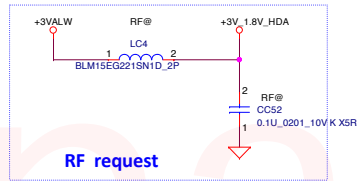
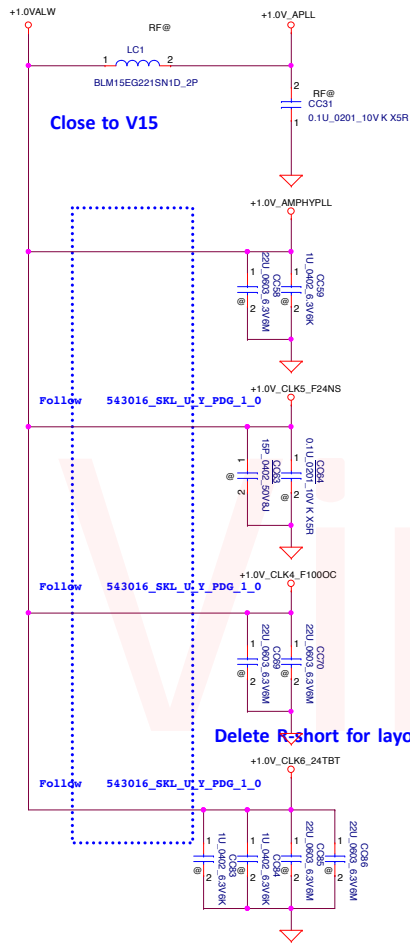
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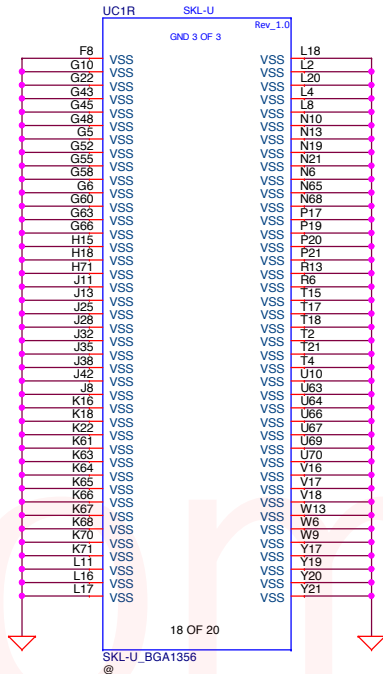
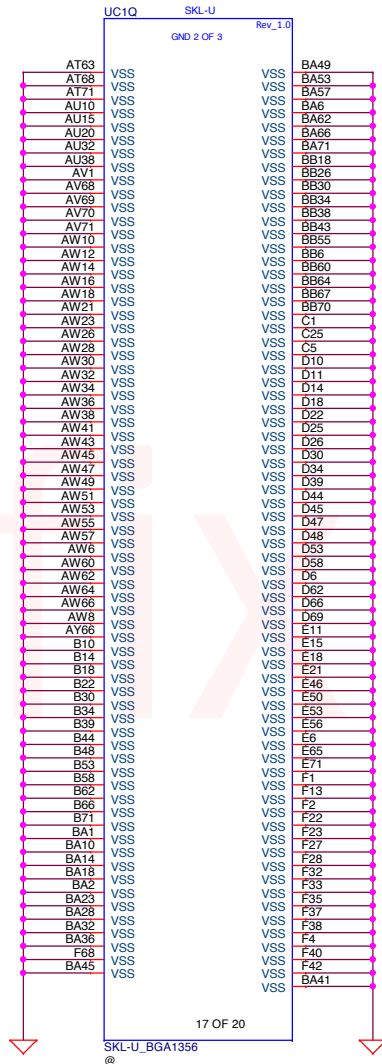
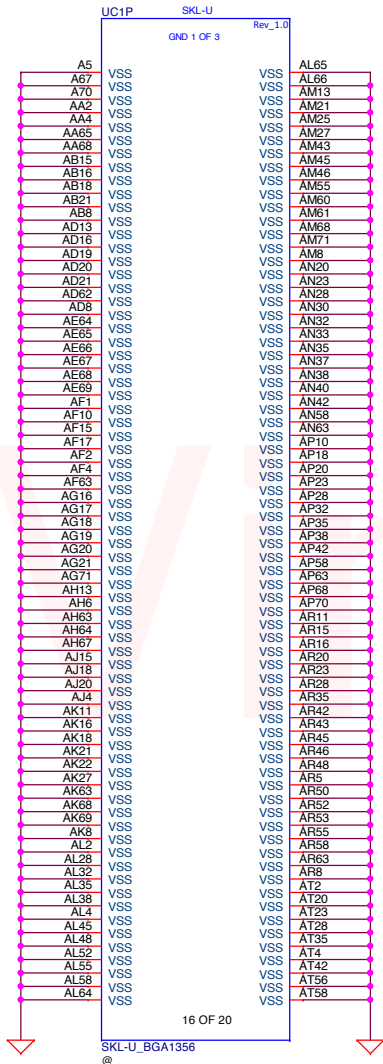


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				Custom	LA-F571P
				Date	Wednesday, November 29, 2017
				Sheet	14 of 45
				Rev	1.0



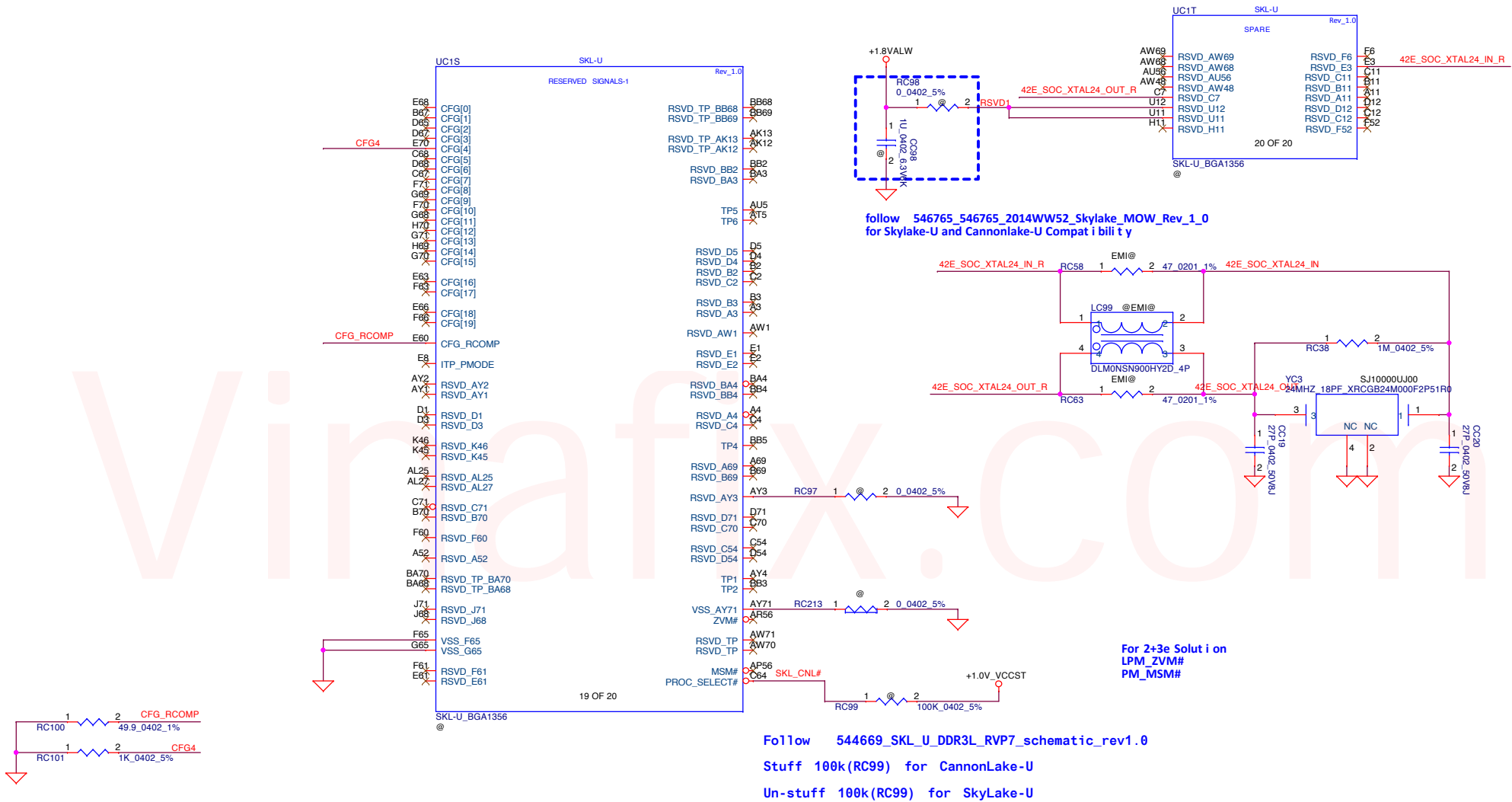






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Issued Date	2017/10/16	Deciphered Date	2020/5/17	Title	
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Size		Document Number		Rev	
Custom		LA-F571P		1.0	
Date:		Wednesday, November 29, 2017		Sheet 16 of 45	





#### Display Port Presence Strap

CFG4

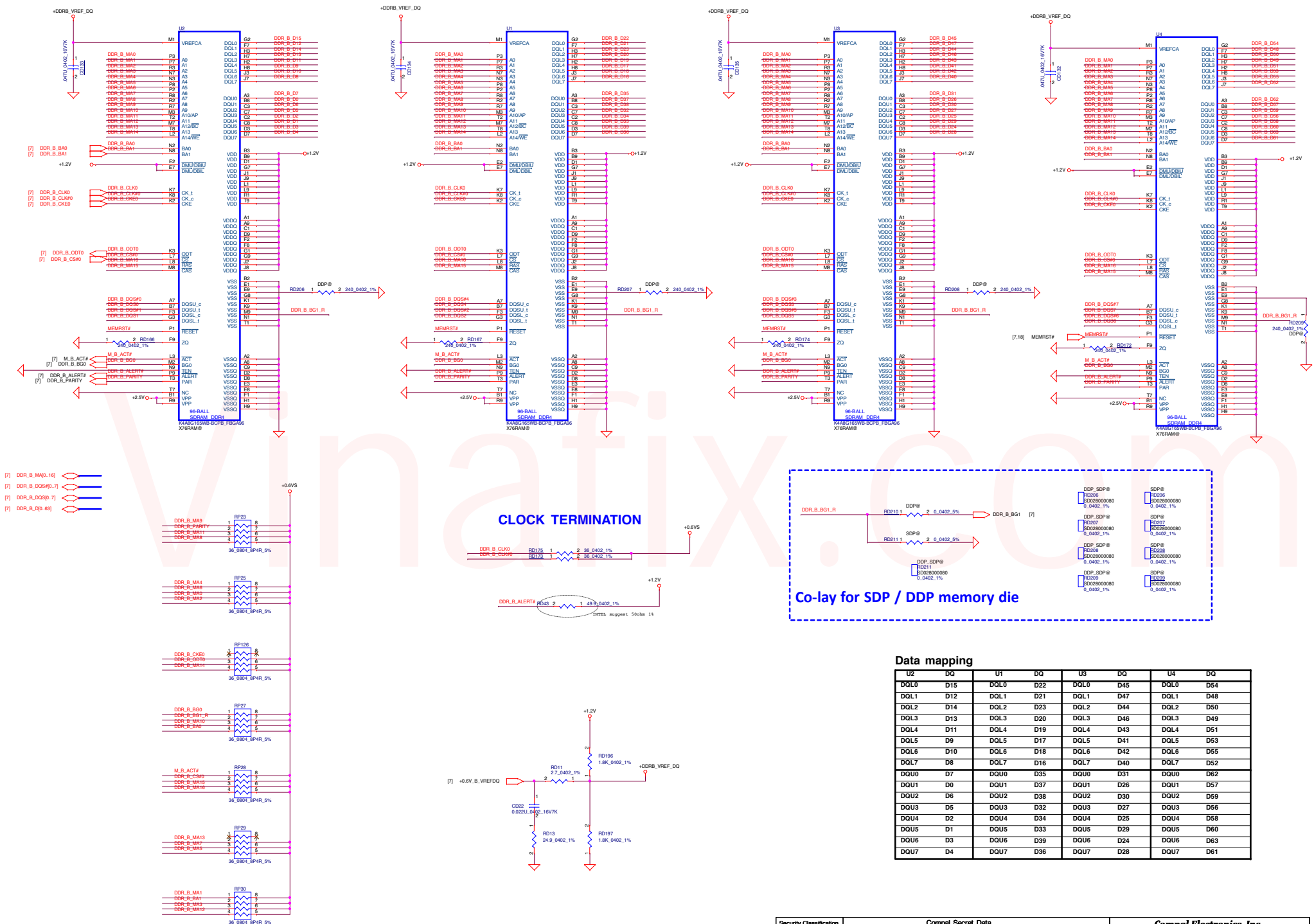
- 1 : Disabled;  
No Physical Display Port at attached Embedded Display Port
- 0 : Enabled;  
An external Display Port device is connected to the Embedded Display Port

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Size	Document	Number	Rev	LA-F571P	
Date:	Wednesday, November 29, 2017	Sheet	17	of	45









**Data mapping**

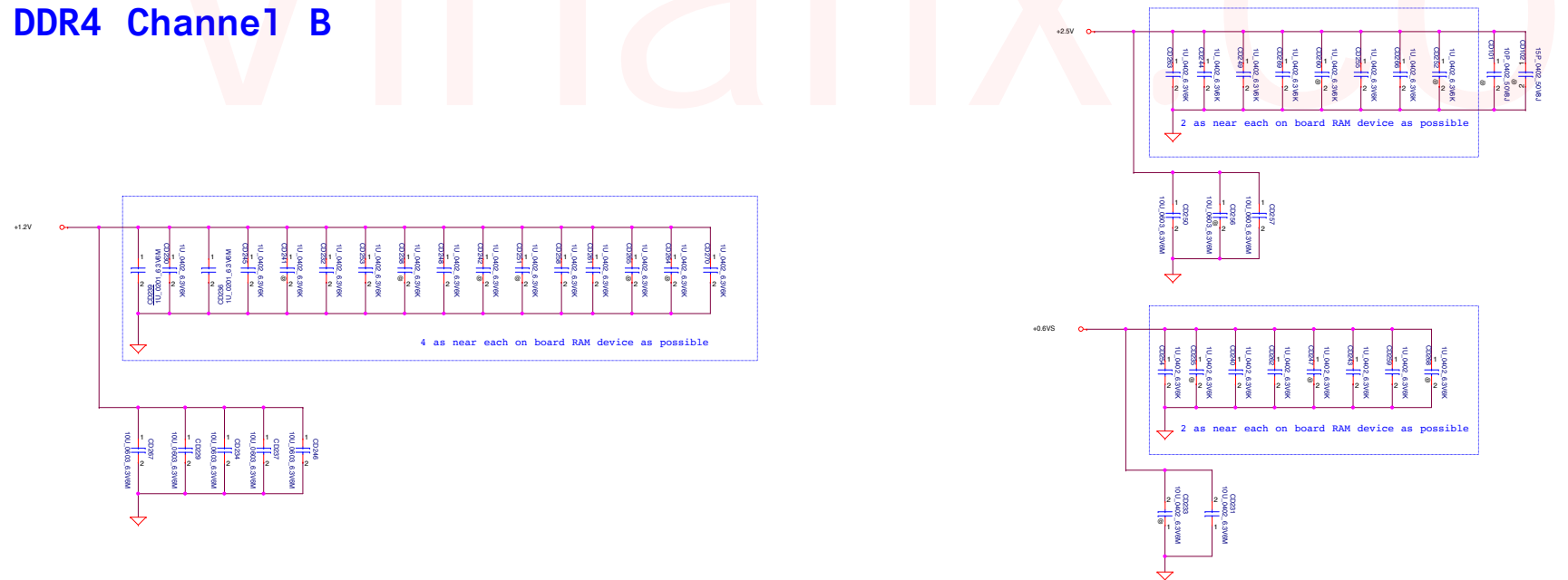
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DQLO	D15	DQLO	D22	DQLO	D45	DQLO	D54
DQL1	D12	DQL1	D21	DQL1	D47	DQL1	D48
DQL2	D14	DQL2	D23	DQL2	D44	DQL2	D50
DQL3	D13	DQL3	D20	DQL3	D46	DQL3	D49
DQL4	D11	DQL4	D19	DQL4	D43	DQL4	D51
DQL5	D9	DQL5	D17	DQL5	D41	DQL5	D53
DQL6	D10	DQL6	D18	DQL6	D42	DQL6	D55
DQL7	D8	DQL7	D16	DQL7	D40	DQL7	D52
DQU0	D7	DQU0	D35	DQU0	D31	DQU0	D62
DQU1	D0	DQU1	D37	DQU1	D26	DQU1	D57
DQU2	D6	DQU2	D38	DQU2	D30	DQU2	D59
DQU3	D5	DQU3	D32	DQU3	D27	DQU3	D56
DQU4	D2	DQU4	D34	DQU4	D25	DQU4	D58
DQU5	D1	DQU5	D33	DQU5	D29	DQU5	D60
DQU6	D3	DQU6	D39	DQU6	D24	DQU6	D63
DQU7	D4	DQU7	D36	DQU7	D28	DQU7	D61



## DDR4 Channel A

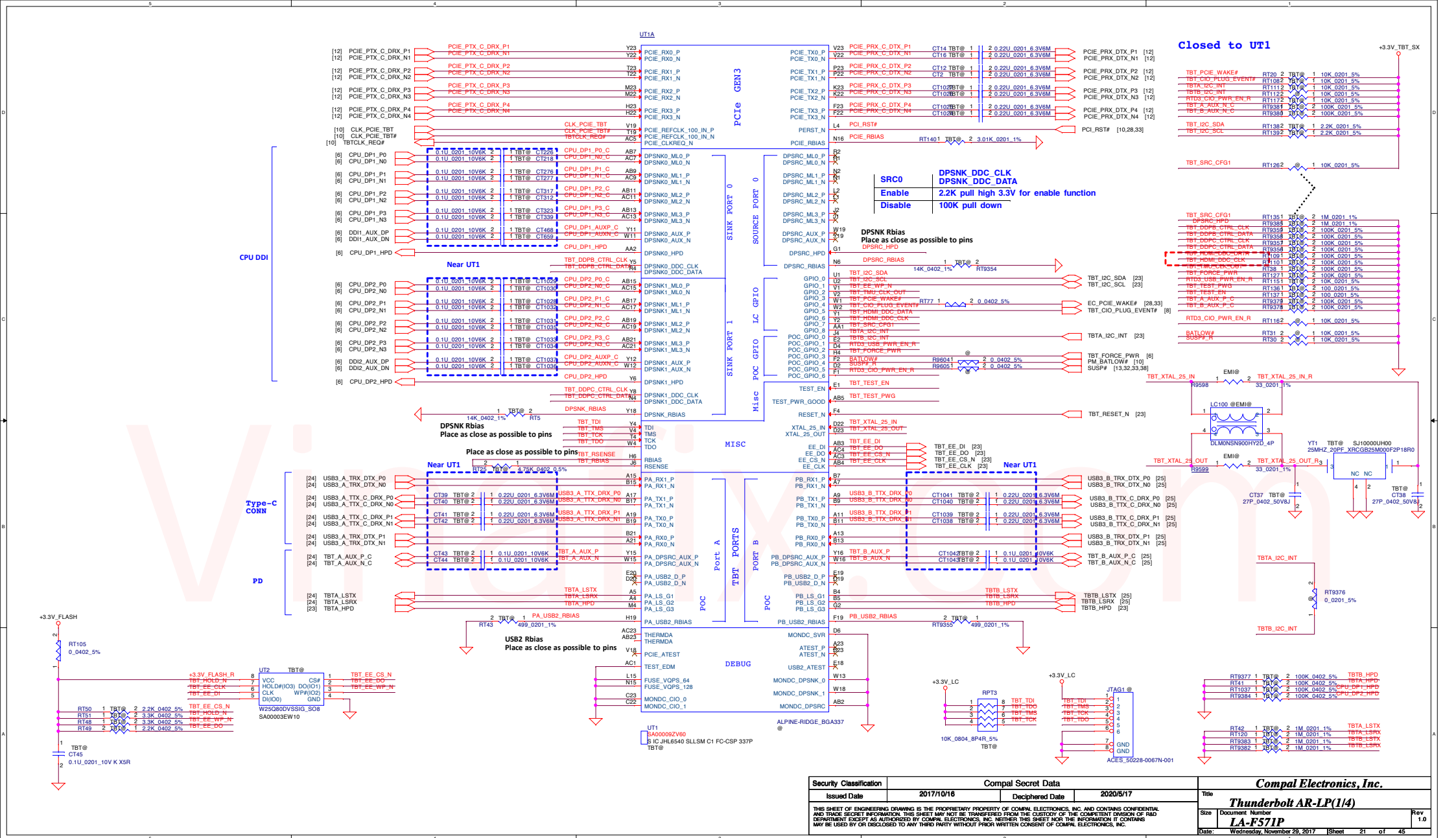


## DDR4 Channel B

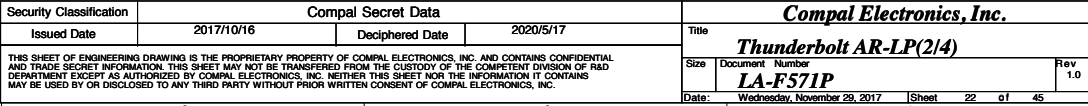


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			Common	<b>LA-F571P</b>	1.0
			Date:	Wednesday, November 29, 2017	
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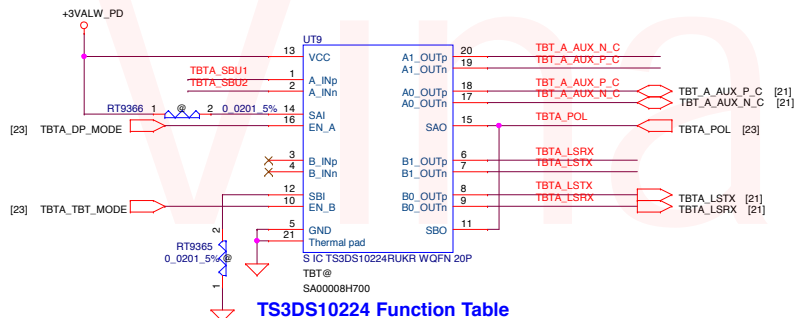
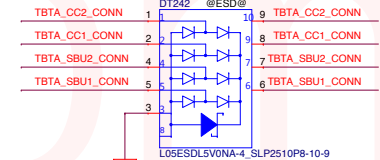
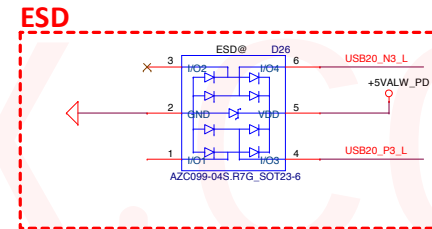
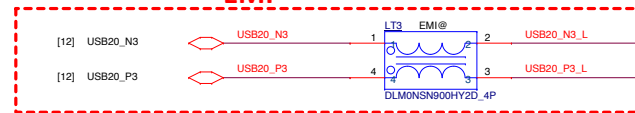
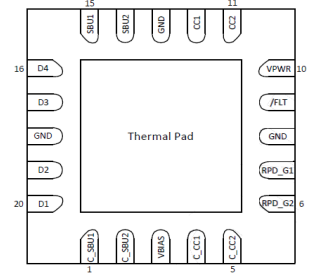
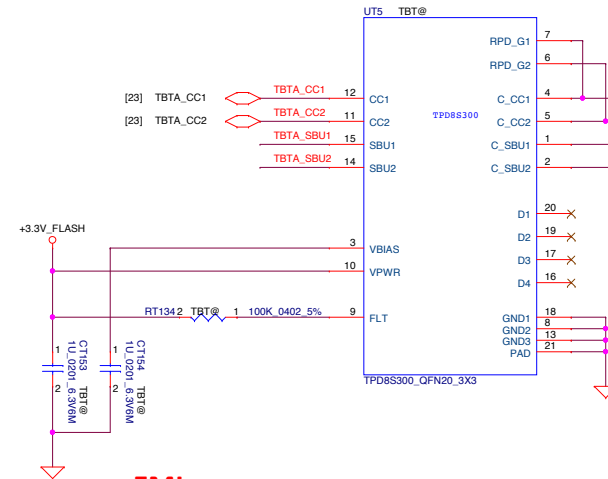
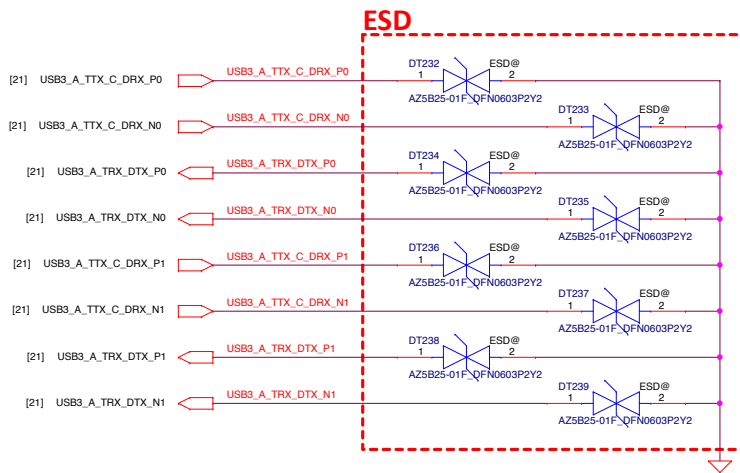










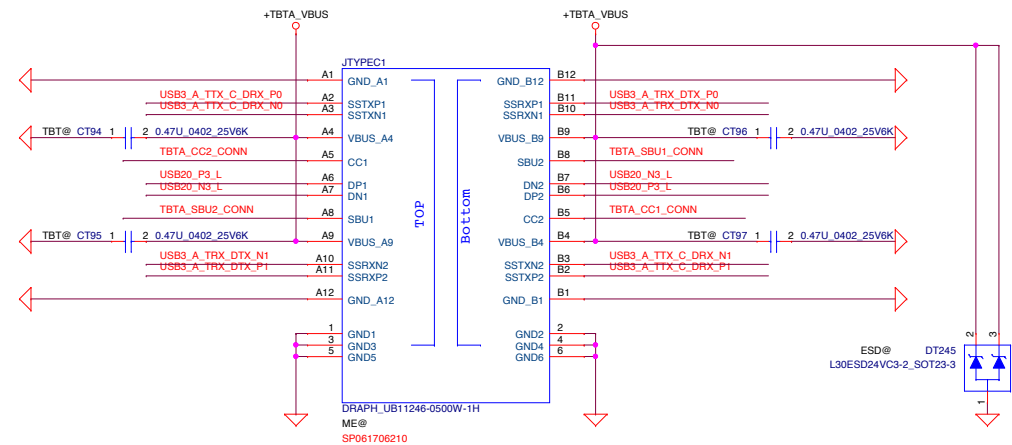


TS3DS10224 Function Table

SBU1	SBU2	(ENA) PA DP Mode	(ENB) PA TBT Mode	(SAO/SBO) PA POL	OUTA0	OUTA1	OUTB0	OUTB1
Hi-Z	Hi-Z	0	0	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
AUX_P	AUX_N	1	0	0	INA	Hi-Z	Hi-Z	Hi-Z
AUX_N	AUX_P	1	0	1	Hi-Z	INA	Hi-Z	Hi-Z
LSTX	LSRX	0	1	0	Hi-Z	Hi-Z	INA	Hi-Z
LSRX	LSTX	0	1	1	Hi-Z	Hi-Z	Hi-Z	INA

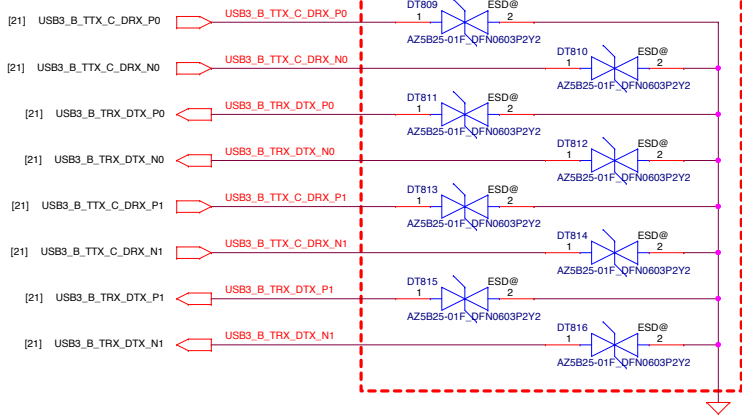
ENA	ENB	OUTA0	OUTA1	OUTB0	OUTB1
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	Hi-Z	EN	EN
1	0	EN	EN	Hi-Z	Hi-Z
1	1	EN	EN	EN	EN

SAI/SAO/SBI/SBO	OUTA0	OUTA1	OUTB0	OUTB1
1 0 0 0	INA	Hi-Z	INA	Hi-Z
1 1 0 1	Hi-Z	INA	Hi-Z	INA

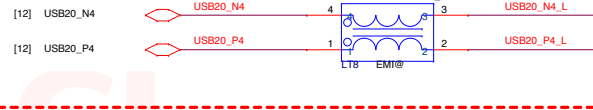




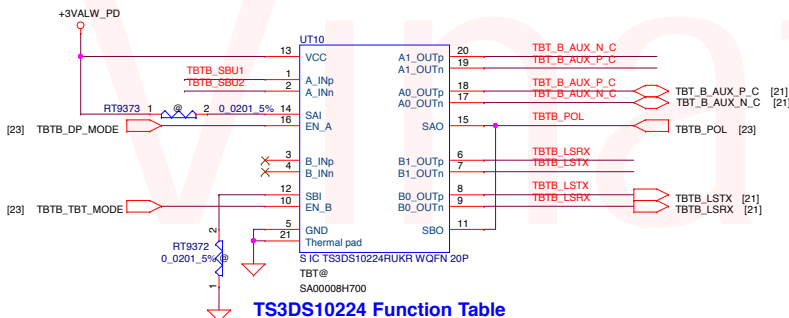
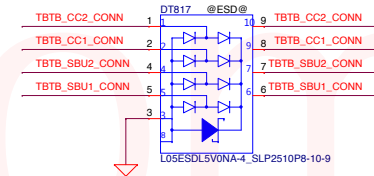
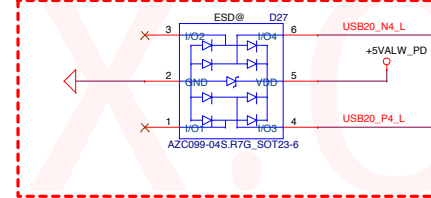
# ESD



# EMI



# ESD



TS3DS10224 Function Table

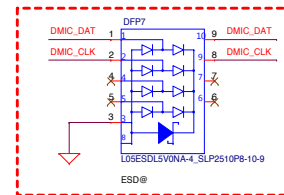
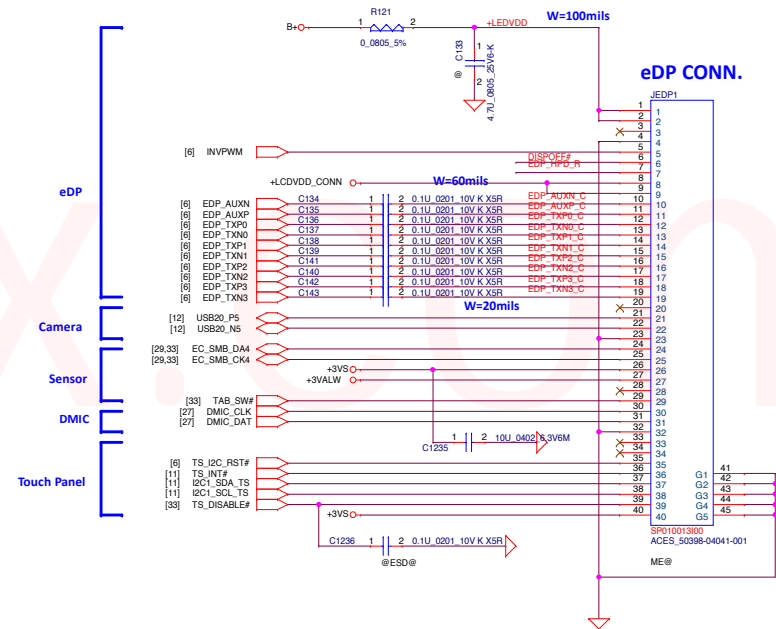
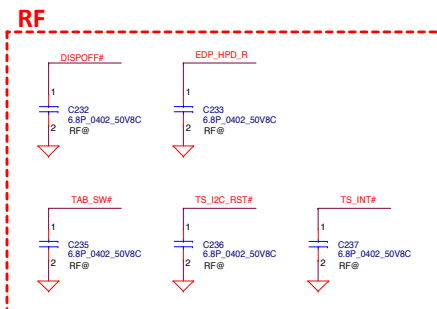
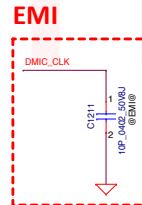
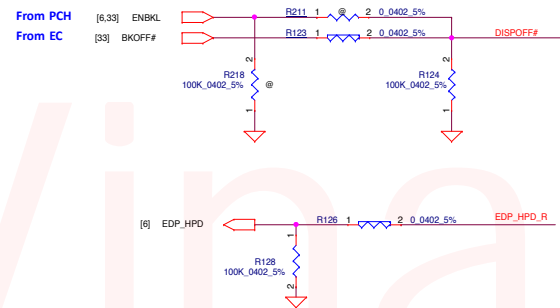
SBU1	SBU2	(ENA) PA DP Mode	(ENB) PA TBT Mode	(SAO/SBO) PA POL	OUTA0	OUTA1	OUTB0	OUTB1
Hi-Z	Hi-Z	0	0	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
AUX_P	AUX_N	1	0	0	INA	Hi-Z	Hi-Z	Hi-Z
AUX_N	AUX_P	1	0	1	Hi-Z	INA	Hi-Z	Hi-Z
LSTX	LSRX	0	1	0	Hi-Z	Hi-Z	INA	Hi-Z
LSRX	LSTX	0	1	1	Hi-Z	Hi-Z	Hi-Z	INA

ENA	ENB	OUTA0	OUTA1	OUTB0	OUTB1
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	Hi-Z	EN	EN
1	0	EN	EN	Hi-Z	Hi-Z
1	1	EN	EN	EN	EN

SAI/SAO/SBI/SBO	OUTA0	OUTA1	OUTB0	OUTB1
1 0 0 0	INA	Hi-Z	INA	Hi-Z
1 1 0 1	Hi-Z	INA	Hi-Z	INA

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				LA-F571P
				Rev 1.0
				Date: Wednesday, November 29, 2017
				Sheet 25 of 45

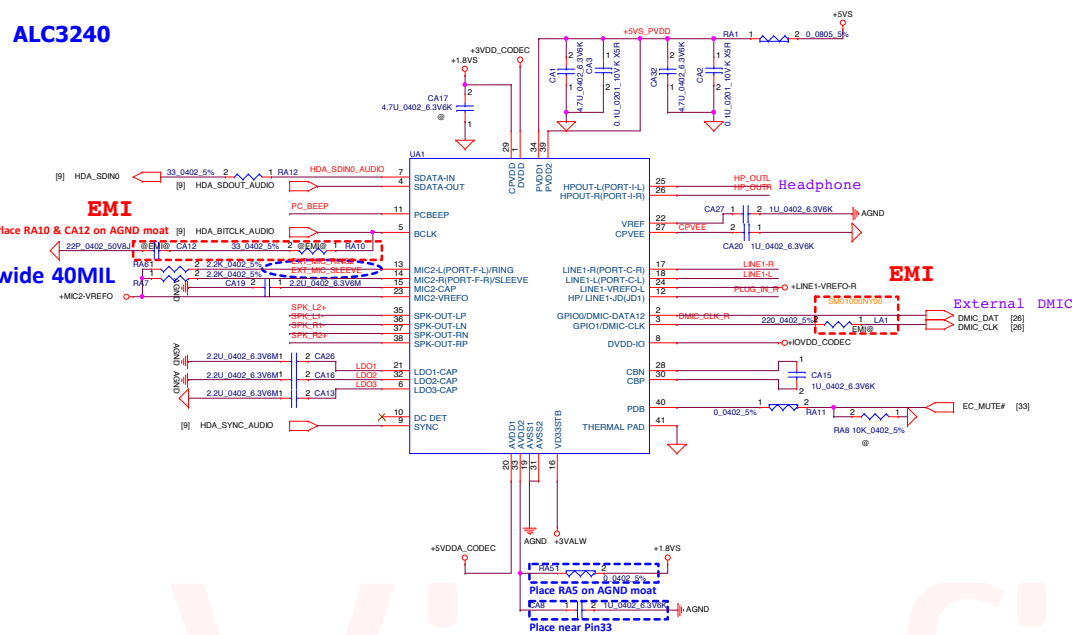




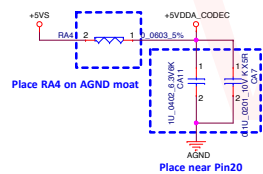
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					LA-F571P
				Date:	Wednesday, November 29, 2017
				Sheet	26 of 45



## ALC3240



**+5VS → +5VDDA\_CODEC**



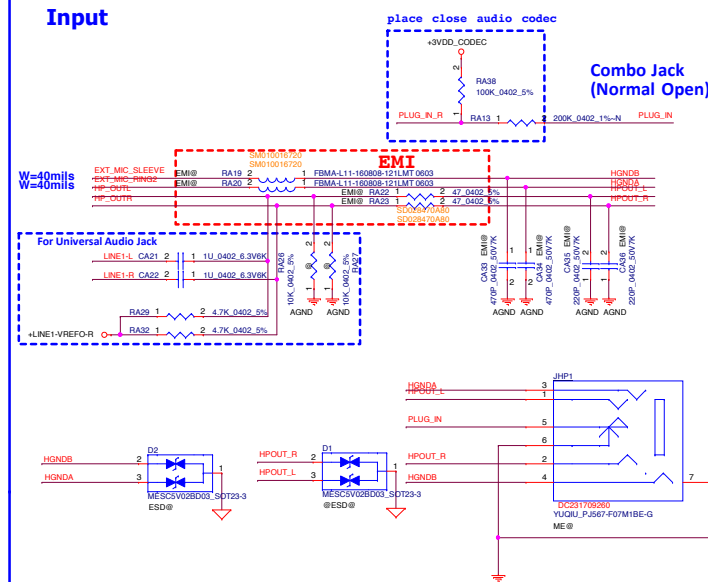
### Each Platform Power Net Support list:

		+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
		1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0-S5)
Intel	Broadwell	V	X	V	V	V
Intel	Skylake	X	V	V	V	V

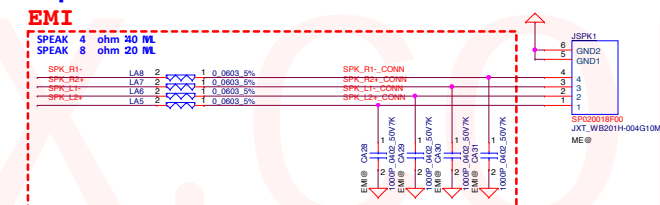
**Each Platf or m HDA li nk Vdt age Support ( R n g):**

	3.3V	1.5V
Intel Broadwell	V (default)	V
Intel Skylake	V (default)	V

## Input

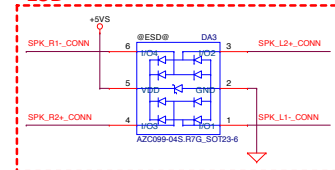


## Output

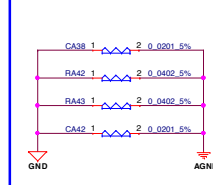


ESD protection needs to be placed near connector side

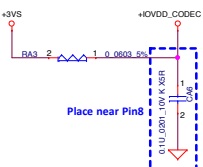
## ESD



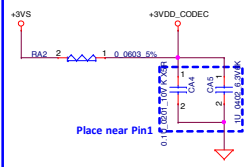
## EMI



## +3VS → +I OVDD\_CODEQ

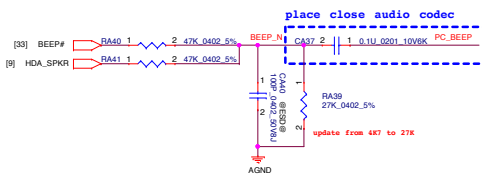


**+3VS → +3VDD\_CODEC**



## PC Beep

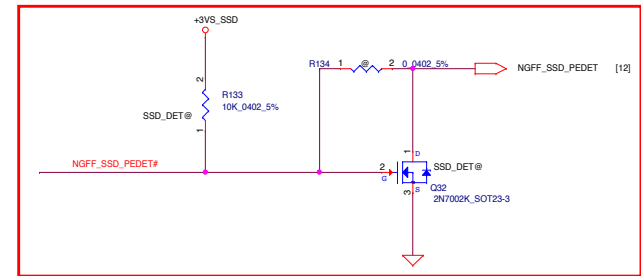
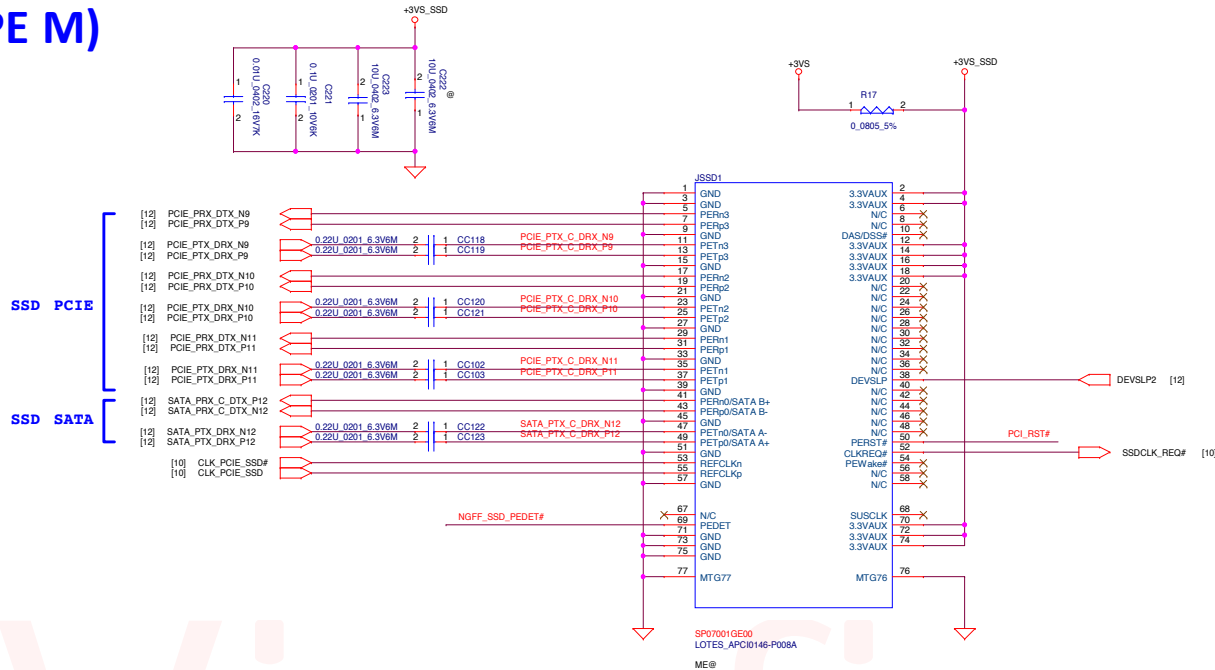
EC Beep  
APU Beep



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				LA-F571P	
Date:				Wednesday, November 29, 2017	Sheet 27 of 45

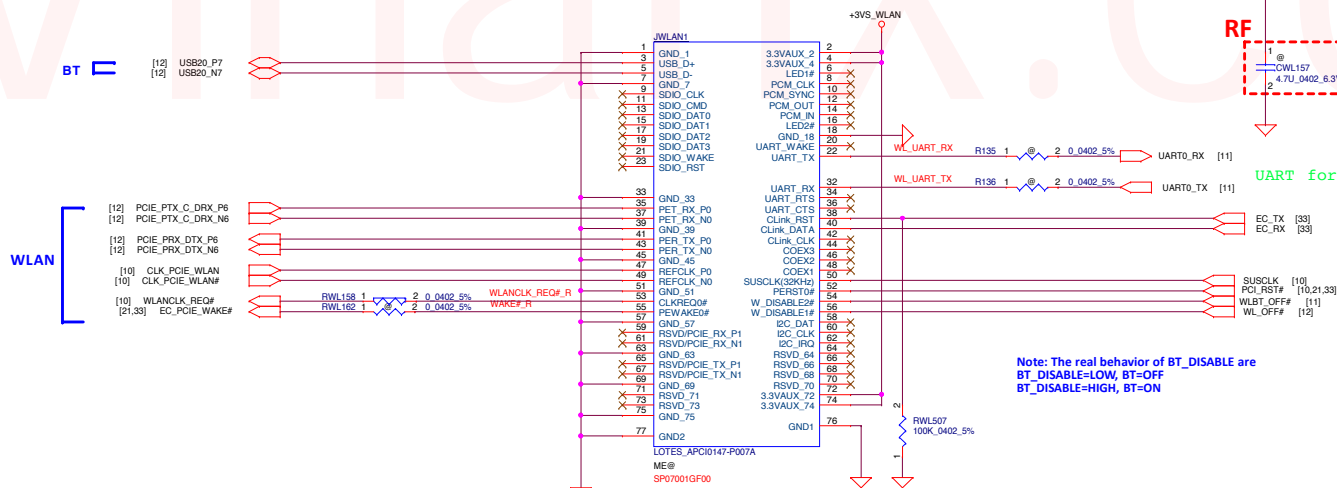


# SSD(TYPE M)



NGFF\_SSD\_PEDET#  
H : PCIE Interface  
L : SATA Interface  
Fellow 543016\_SKL\_U\_Y\_PDG\_0\_9

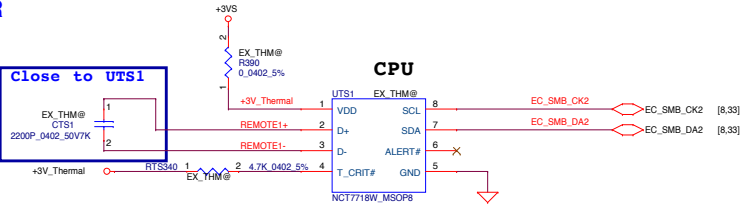
# NGFF WLAN /BT(TYPE E)



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Size	C	Document Number	LA-F571P	Rev 1.0
Date:	Wednesday, November 29, 2017	Sheet	28	of 45

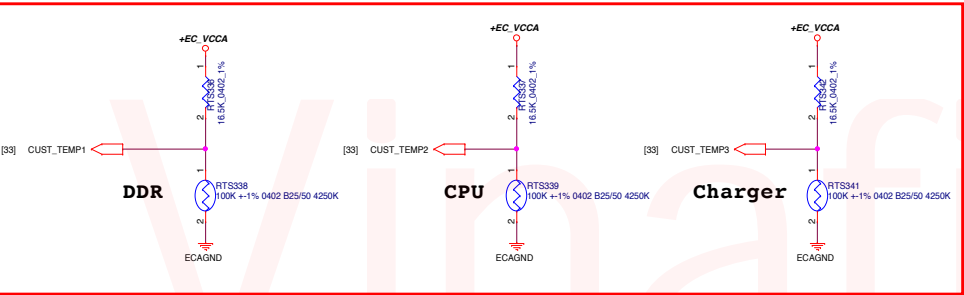
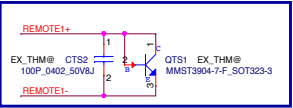


THERMISTOR

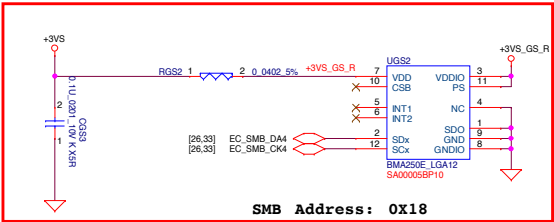


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Trace width/space:10/10 mil  
Trace length:<8"

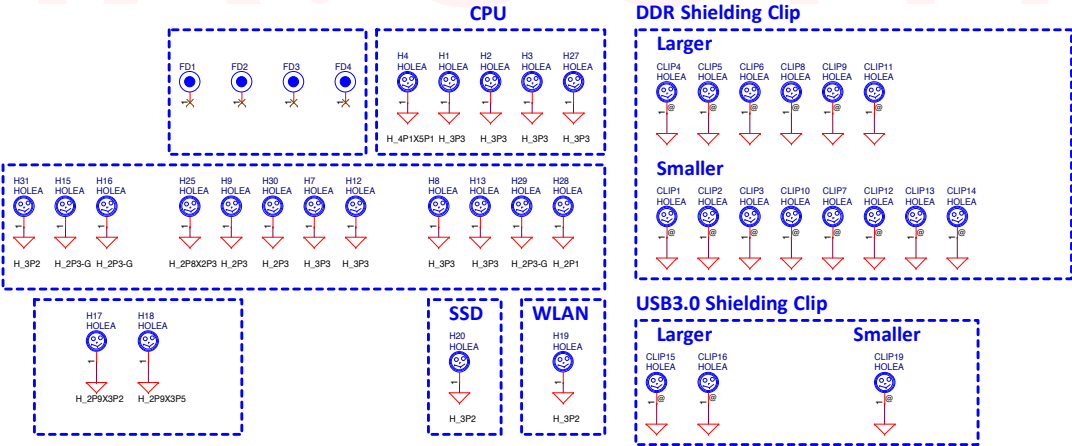
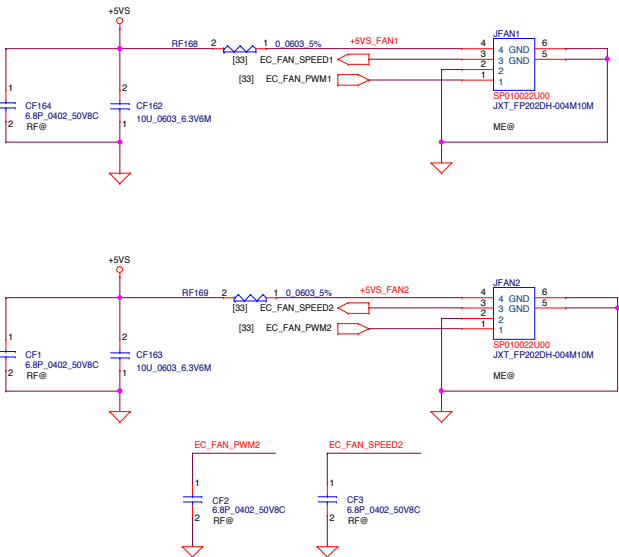
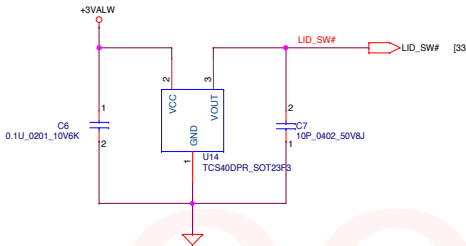
DDR



G-Sensor



Hall Sensor



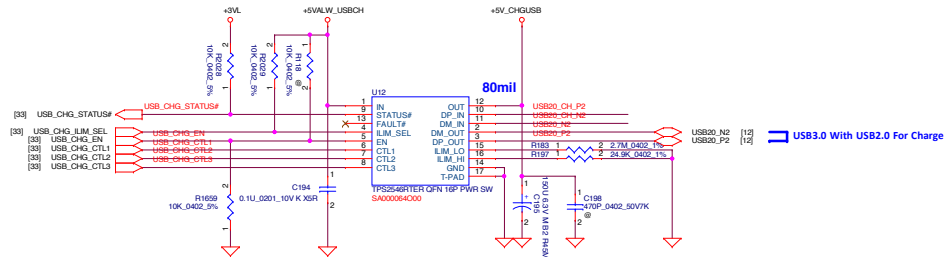
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Issued Date	2017/10/16	Deciphered Date	2020/5/17	Title
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Size	Document Number	LA-F571P		Rev 1.0
Date: Wednesday, November 28, 2017		Sheet 29 of 45		



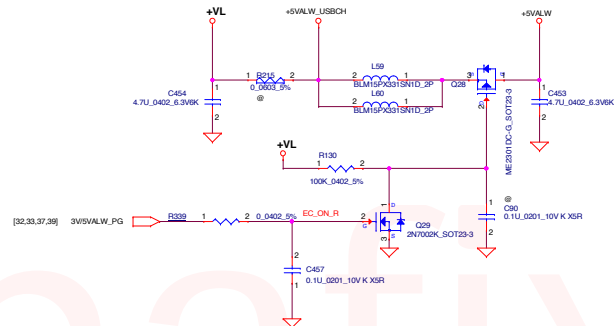
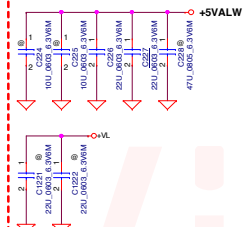




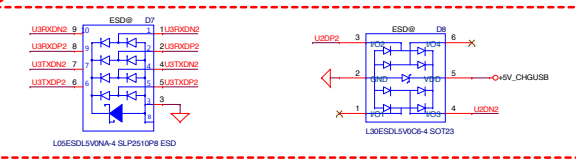
## USB Charger



Down USB charger Iout ripple  
must under 20mA on DC S5



**ESD**

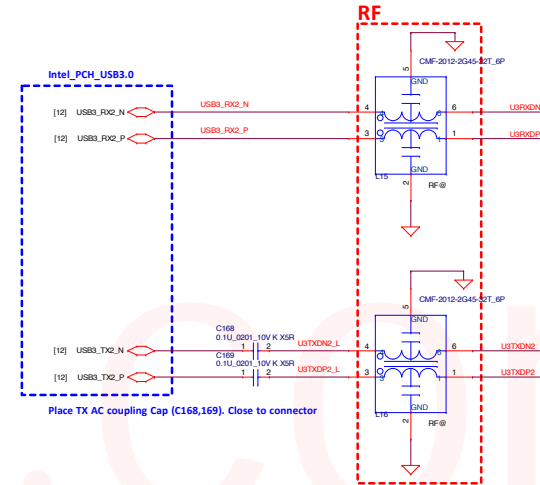
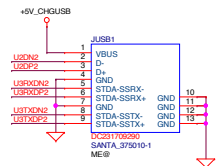


## USB3.0\_Port



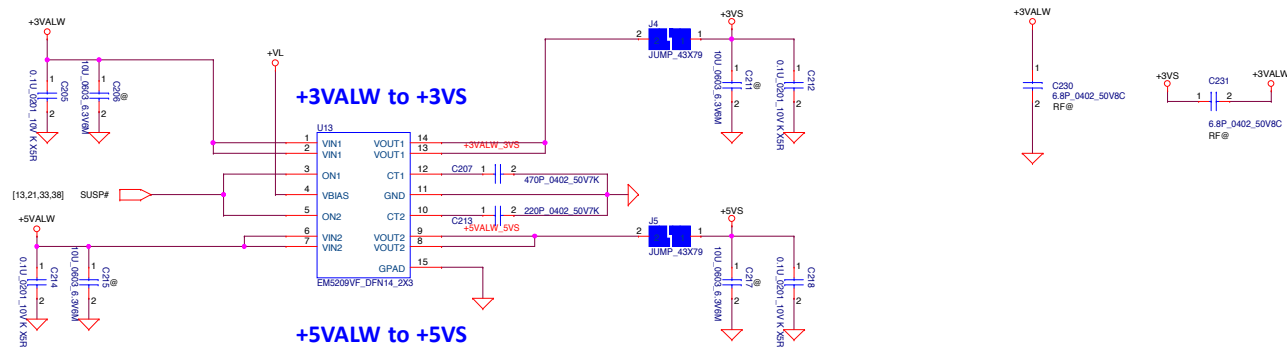
USB3.0 CONN (for charger)

W=80mils



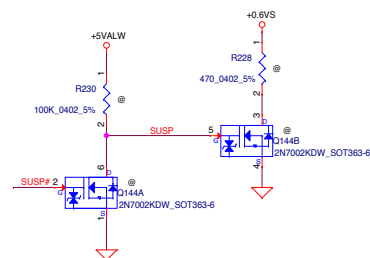
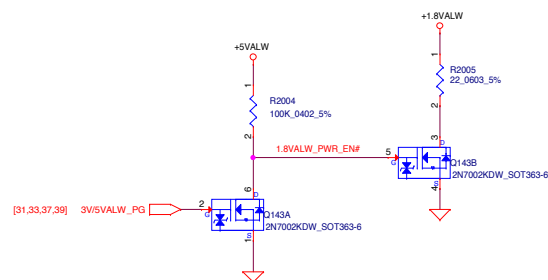
Security Classification	Compal Secret Data			Title		
Issued Date	2017/10/16	Deciphered Date	2020/5/17	USB2 / USB3 / FP / IO Board		
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**For +1.8V<sub>ALW</sub> Discharge**

**For +0.6VS Discharge**

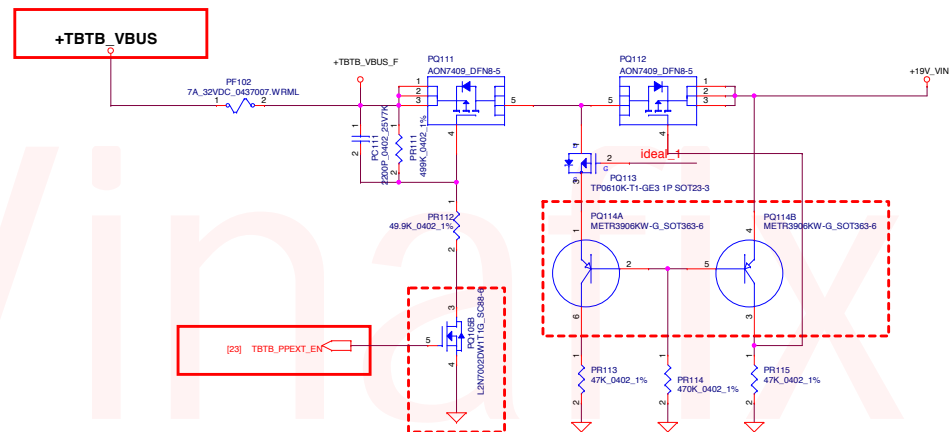


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				Size C	Document Number	Rev 1.0
				LA-F571P		
				Date	Wednesday, November 29, 2017	Sheet 32 of 45



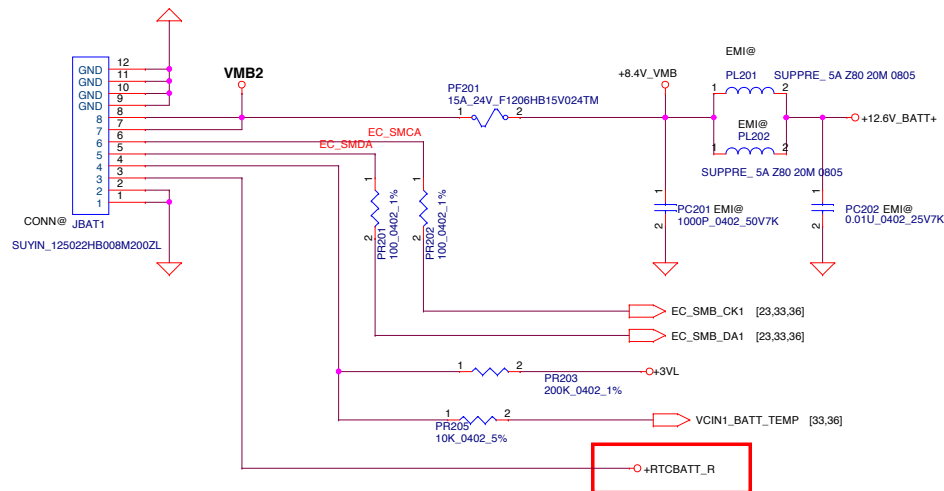




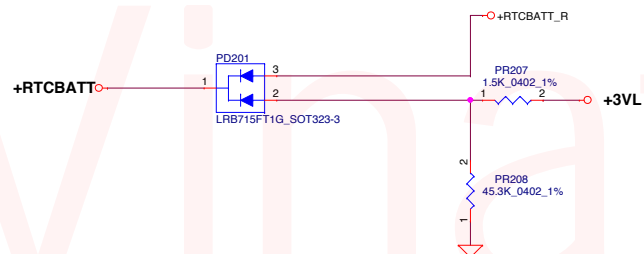
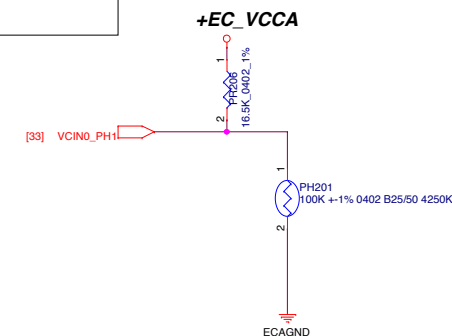


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				Size	Document Number	Rev
				Custom	LA-E5513P	1.0
				Date:	Wednesday, November 28, 2017	Sheet 34 of 45





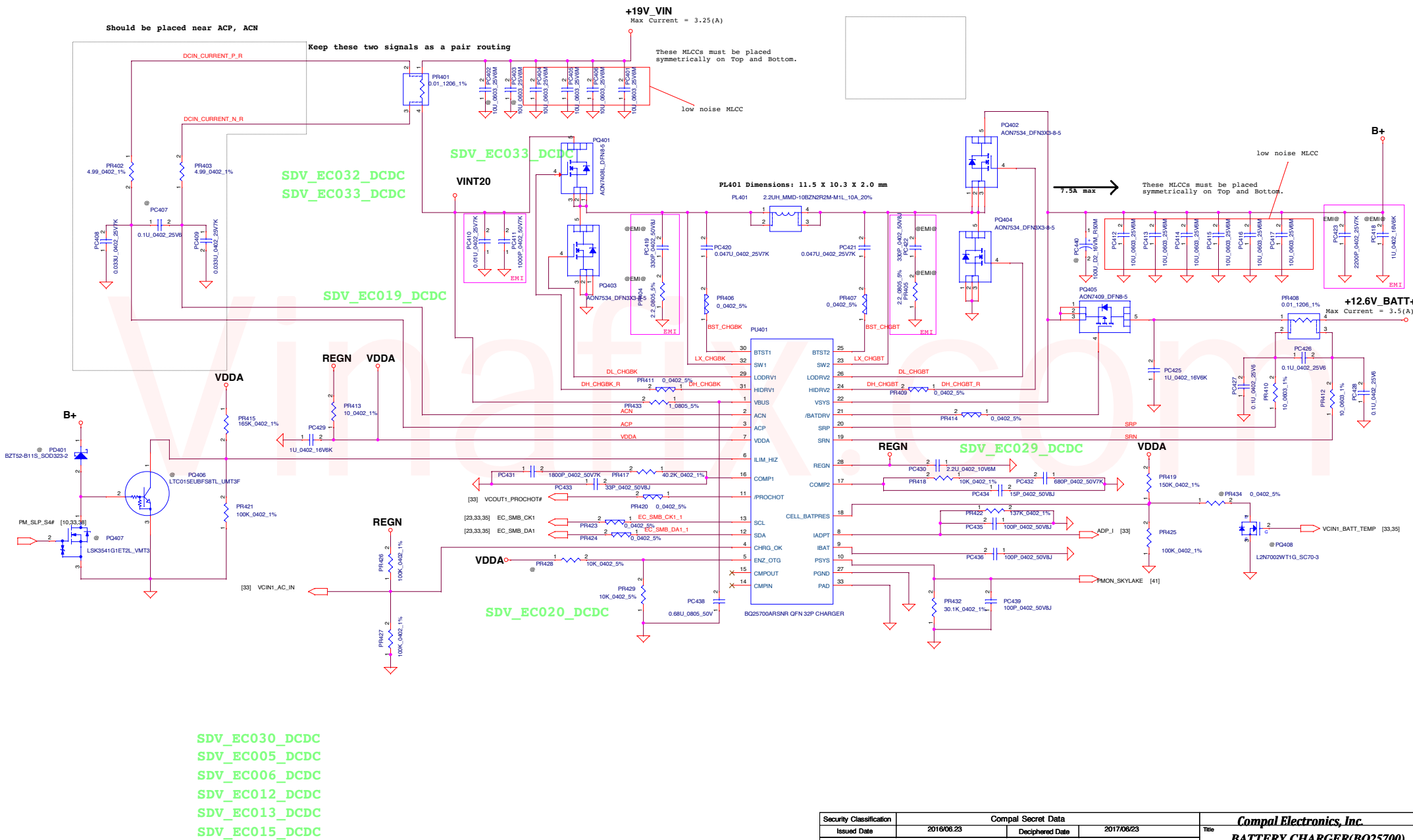
**PH201 under CPU bottom side :**  
**CPU thermal protection at 93 +3 degree C**  
**Recovery at 56 +3 degree C**



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2016/06/23		Deciphered Date		2017/06/23		Title	
										PWR- BATTERY CONN/OTP	
										Size Document Number	
										LAE551P	
										Rev	
										1.0	
										Date: Wednesday, November 29, 2017	
										Sheet 35 of 45	

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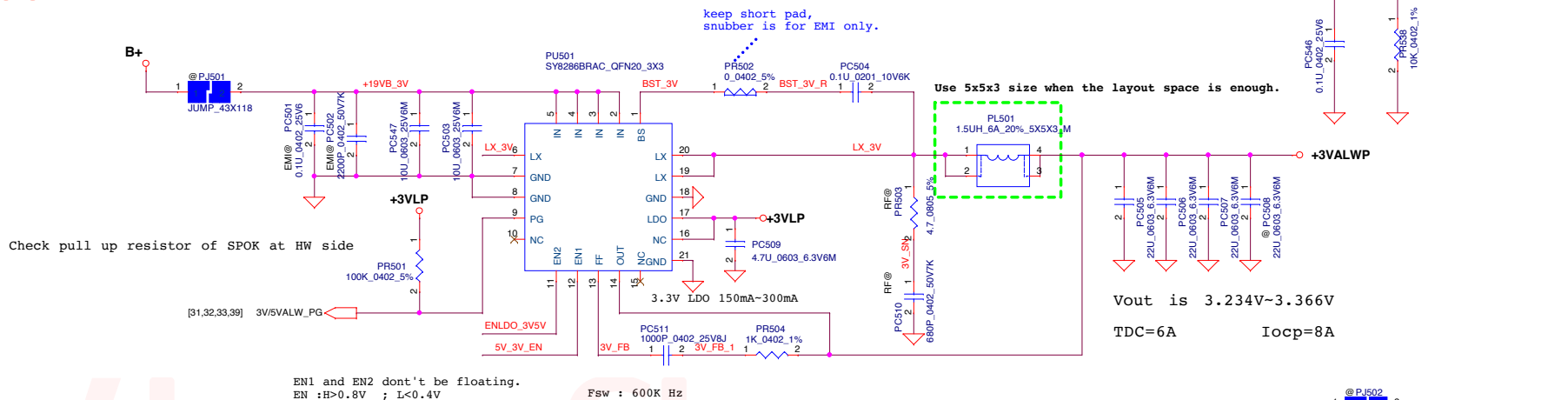


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Compal Electronics, Inc. <b>BATTERY CHARGER(BQ25700)</b>				Rev
Size Document Number Custom <b>LA-E5513P</b>				Rev
Date: Wednesday, November 23, 2017				Rev
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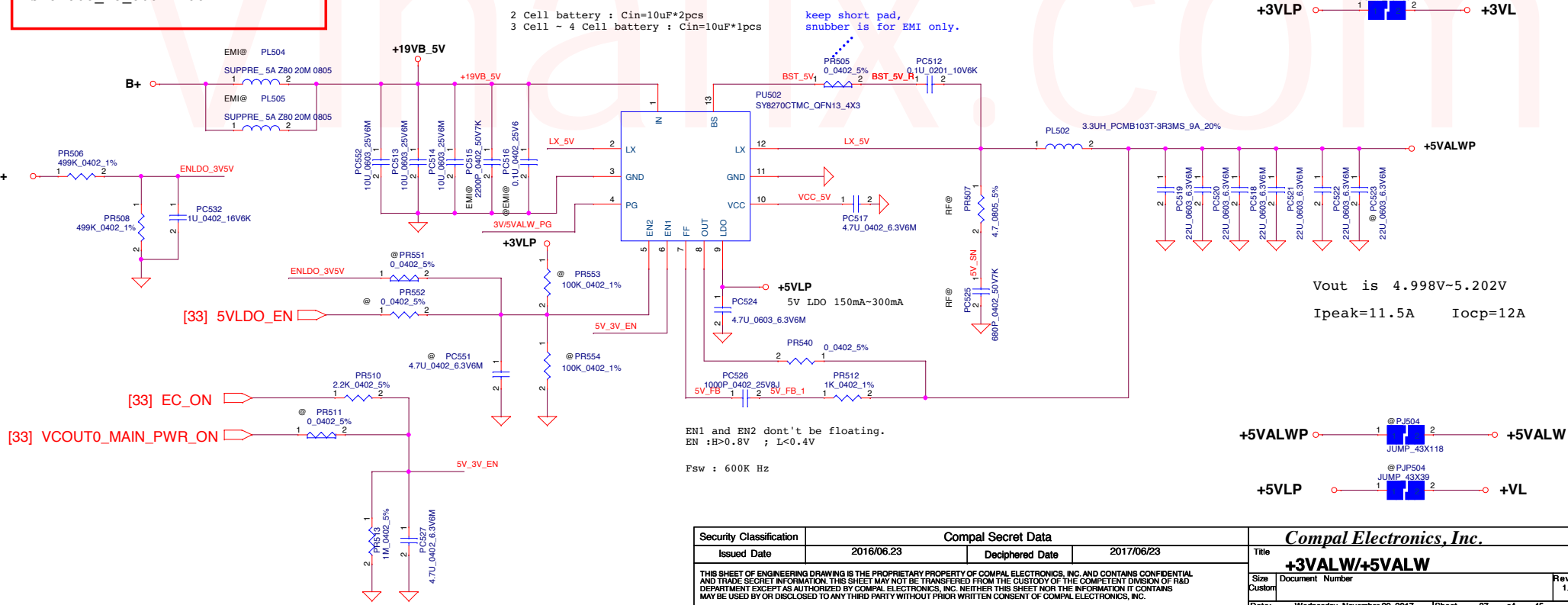


SY8286B\_V3\_single.mdd  
SY8286B\_V3\_dual.mdd

# Vinafix.com

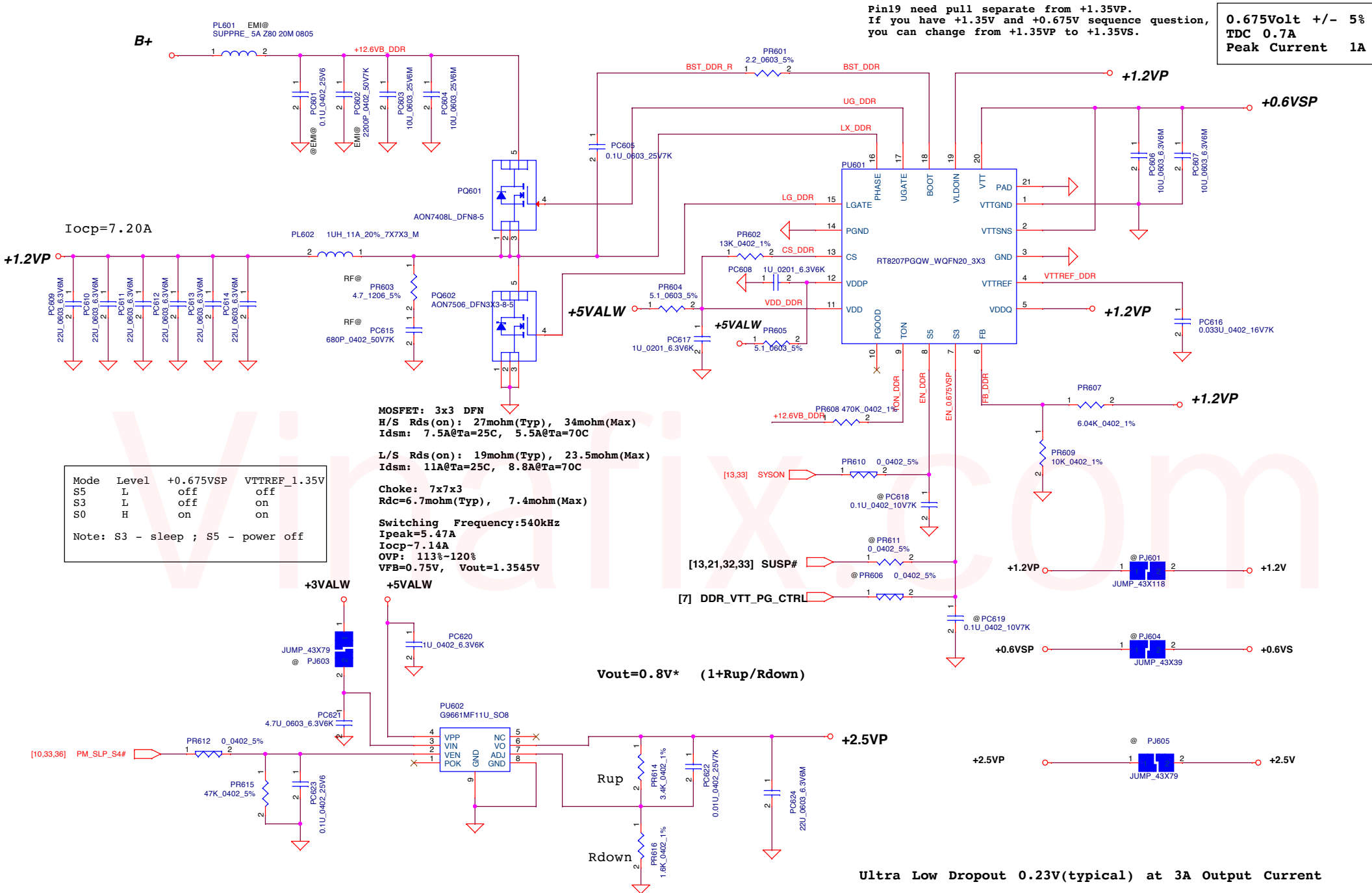


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SY8286C_V3_single.mdd
SY8286C_V3_dual.mdd
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Pin19 need pull separate from +1.35VP.  
If you have +1.35V and +0.675V sequence question,  
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%  
TDC 0.7A  
Peak Current 1A

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN  
H/S Rds(on): 27mohm(Typ), 34mohm(Max)  
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 19mohm(Typ), 23.5mohm(Max)  
Idsm: 11A@Ta=25C, 8.8A@Ta=70C

Choke: 7x7x3  
Rdc=6.7mohm(Typ), 7.4mohm(Max)

Switching Frequency:540kHz  
Ipeak=5.47A  
Iocp=7.14A  
OVP: 113%~120%  
VFB=0.75V, Vout=1.3545V

$V_{out} = 0.8V \times (1 + \frac{R_{up}}{R_{down}})$

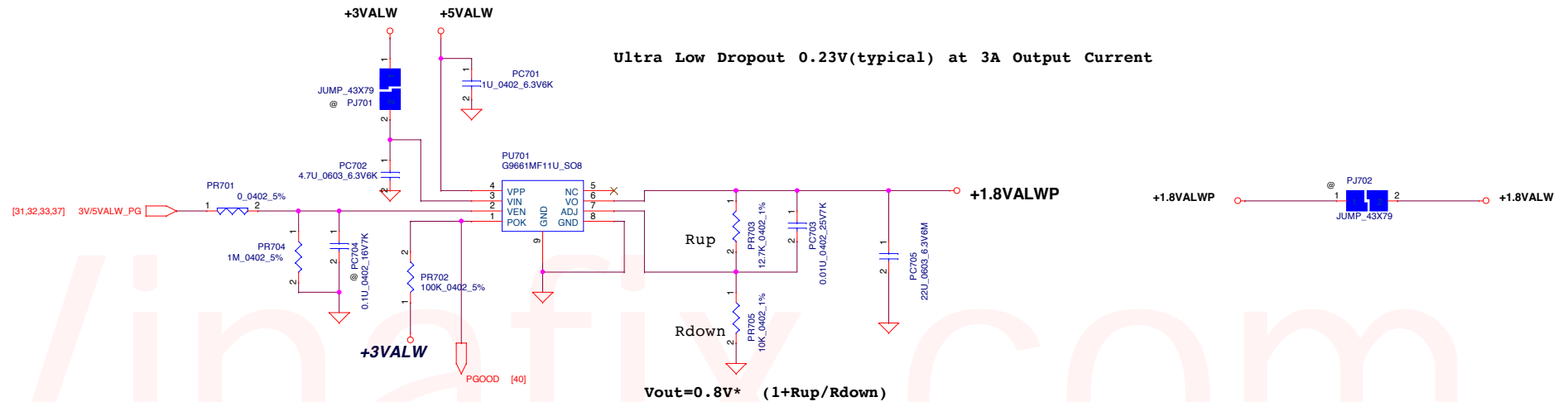
Ultra Low Dropout 0.23V(typical) at 3A Output Current

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Custom				1.0	
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# Module model information

APL5930\_V2.mdd

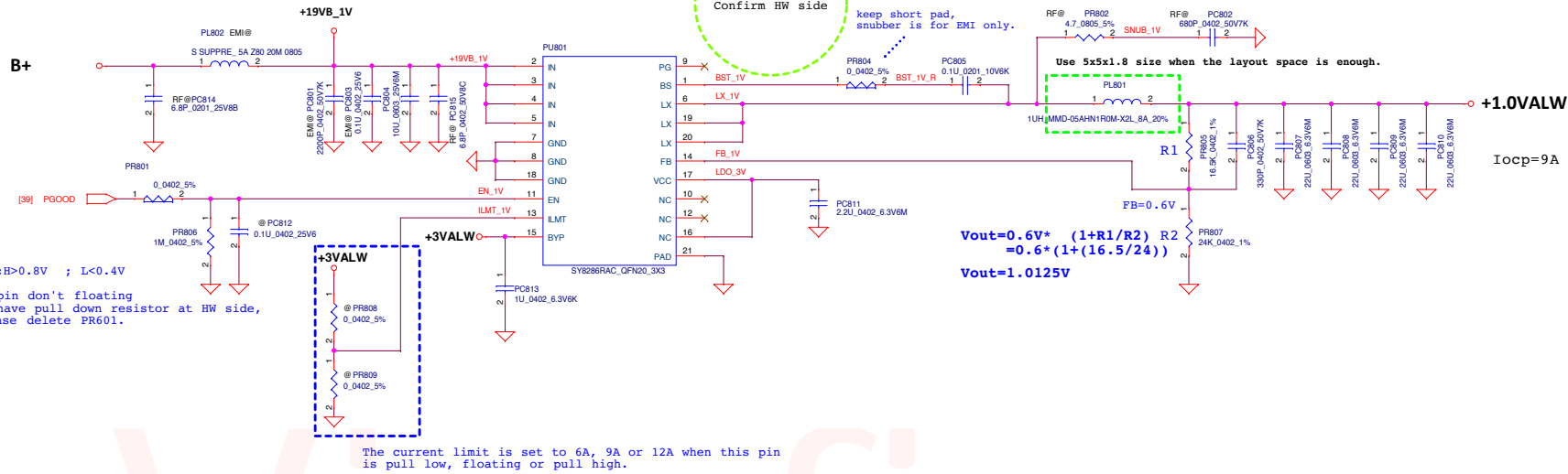


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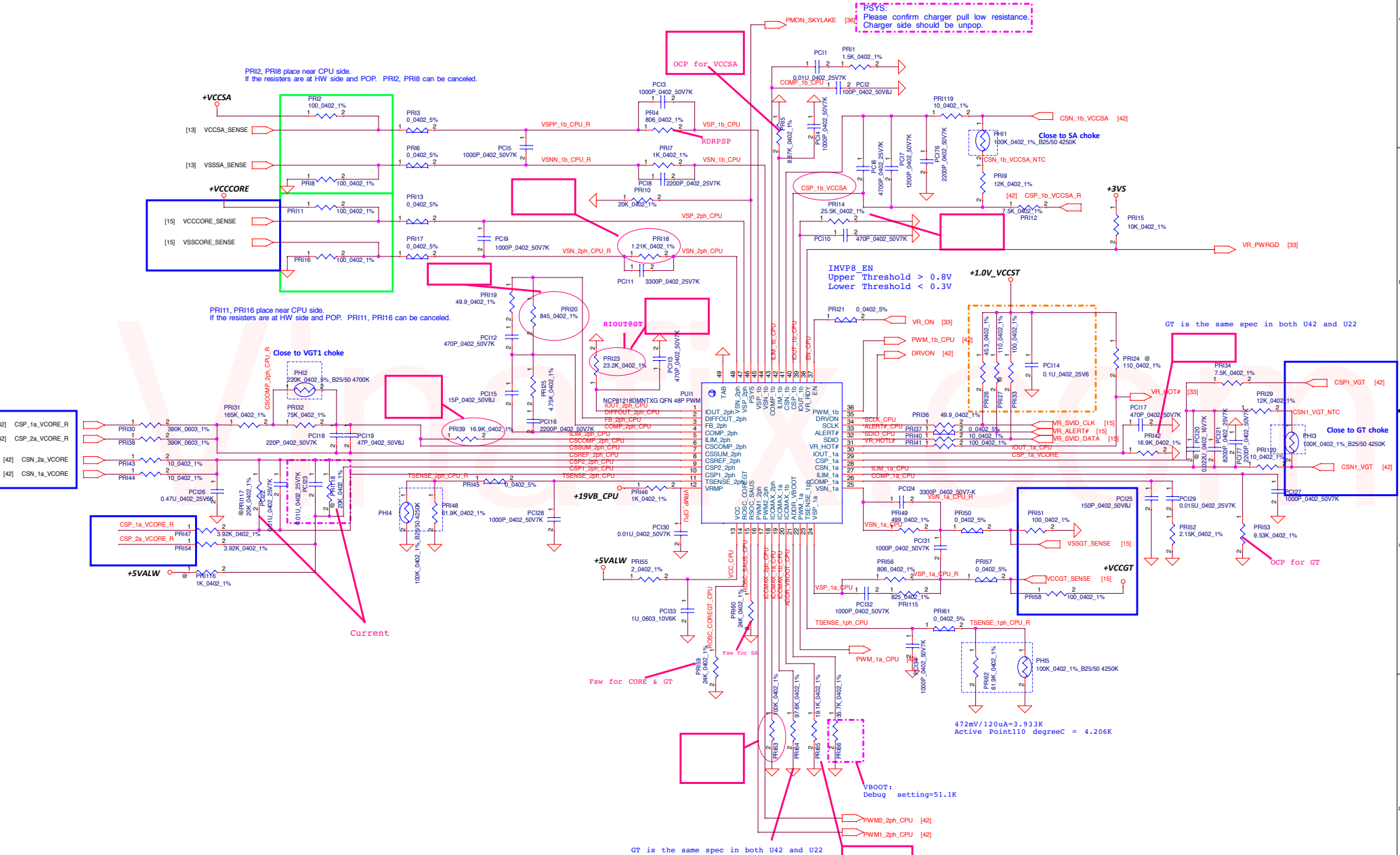
# Module model information

SY8286\_V1\_single.mdd  
SY8286\_V1\_dual.mdd



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Size	Document Number	Rev		1.0
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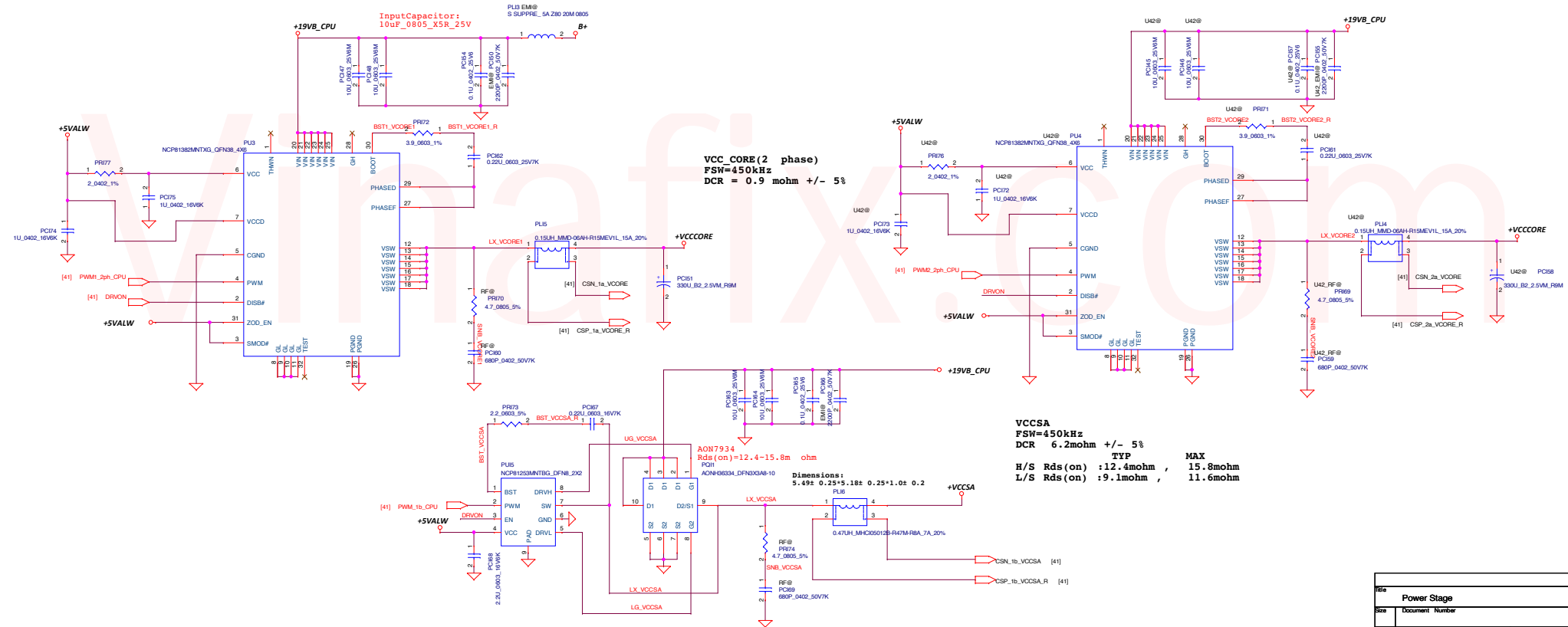
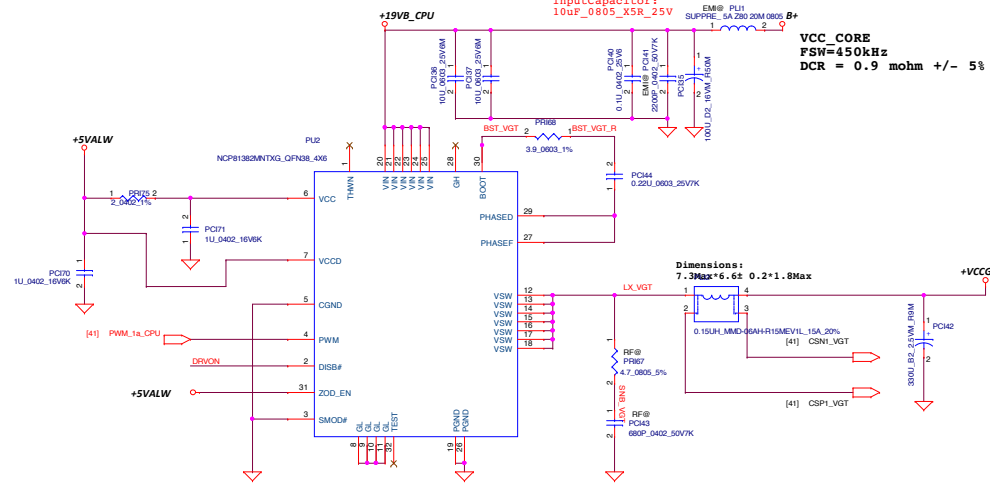




Title			
NCP81218(U22&U42)			
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## CPU POWER STAGES



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Power Stage		
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VCC\_CORE  
22U\_0603 \* 16 pcs +1U\_0201\*40 pcs  
10U\_0402 \* 24 pcs

VCC\_GT CAP  
22U\_0603 \* 14 pcs +1U\_0201\*8 pcs  
10U\_0402 \* 31 pcs

